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Motion Estimation and Error Detection and Correction with EDDR Techniques and Testing Applications

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Abstract: ***In this paper we propose with the help of Digital image/video processing application the MPEG and AME are unable to correct the given critical code when they are in motion for that purpose we propose the role of motion estimation (ME) in a video coder, While focusing on the testing of ME in a video coding system, the paper presents an error detection and data recovery (EDDR) design, based on the residue-and-quotient (RQ) code, to embed into ME for video coding testing applications. An error in a key component of a ME can be detected and recovered effectively by using the proposed EDDR design. Experimental results indicate that the proposed EDDR design for ME testing is the best method for the error detection and correction with the EDDR within acceptable area overhead and timing penalty. Importantly, the proposed EDDR design performs satisfactorily in terms of throughput and reliability for ME testing applications.***

Keywords: Area overhead, data recovery, error detection, motion estimation, reliability, residue-and-quotient (RQ) code.

1. Introduction

Advances in semiconductors, digital signal processing, and communication technologies have made multimedia applications more flexible and reliable. A good example is the H.264 video standard, also known as MPEG-4 Part 10 Advanced Video Coding, which is widely regarded as the next generation video compression standard [1], [2]. Video compression is necessary in a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding systems, a ME is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. Additionally, while performing up to 60%–90% of the computations encountered in the entire coding system, a ME is widely regarded as the most computationally intensive of a video coding system [3]. AME generally consists of PEs with a size of 4 X 4. However, accelerating the computation speed depends on a large PE array, especially in high-resolution devices with a large search range such as HDTV [4]. Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME. Moreover, although the advance of VLSI technologies facilitates the integration of a large number of PEs of a ME into a chip, the logic-per-pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing on the chip. As a commercial chip, it is absolutely necessary for the ME to introduce design for testability (DFT) [5]–[7]. DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods rely on reconfiguration of a circuit under test (CUT) to improve testability. While DFT approaches enhance the testability of circuits, advances in sub-micron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world. BIST for the ME does not expensive test equipment, ultimately lowering test costs [8]–[10]. Moreover, BIST can generate test simulations and analyze test responses without outside support, subsequently streamlining the testing and diagnosis of digital systems. However, increasingly complex density of circuitry requires that the built-in testing approach not only detect faults but also specify their locations for error correcting. Thus, extended schemes of BIST referred to as built-in self-diagnosis [11] and built-in self-correction [12]–[14] have been developed recently. While the extended BIST schemes generally focus on memory circuit, testing-related issues of video coding have seldom been addressed. Thus, exploring the feasibility of an embedded testing approach to detect errors and recover data of a ME is of worthwhile interest. Additionally, the reliability issue of numerous PEs in a ME can be improved by enhancing the capabilities of concurrent error detection (CED) [15], [16]. The CED approach can detect errors through conflicting and undesired results generated from operations on the same operands. CED can also test the circuit at full operating speed without interrupting a system. Thus, based on the CED concept, this work develops a novel EDDR architecture based on the RQ code to detect errors and recovery data in PEs of a ME and, in doing so, further guarantee the excellent reliability for video coding testing applications. The rest of this paper is organized as follows. Section II describes the mathematical model of RQ code and

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the corresponding circuit design of the RQ code generator (RQCG). Section III then introduces the proposed EDDR architecture, fault model definition, and test method. Next, Section IV evaluates the performance in area overhead, timing penalty, throughput and reliability analysis to demonstrate the feasibility of the proposed EDDR architecture for ME testing applications. Conclusions are finally drawn in Section V.

2. Proposed EDDR Architecture Design

Fig. 1 shows the conceptual view of the proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT.

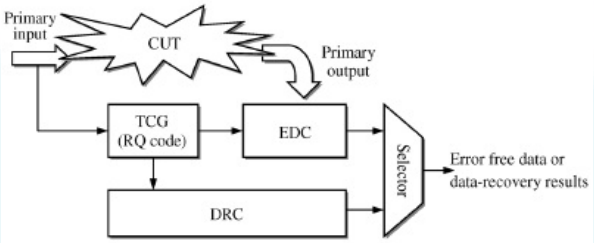

Figure 1: The proposed EDDR architecture

The test code generator (TCG) in Fig. 1 utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data. This work adopts the systolic ME [19] as a CUT to demonstrate the feasibility of the proposed EDDR architecture. A ME consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. A PE generally consists of two ADDs (i.e. an 8-b ADD and a 12-b ADD) and an accumulator (ACC). Next, the 8-b ADD (a pixel has 8-b data) is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications [20]. Notably, some registers and latches may exist in ME to complete the data shift and storage. Fig. 2 shows an example of the proposed EDDR circuit design for a specific of a ME. The fault model definition, RQCG-based TCG design, operations of error detection and data recovery, and the overall test strategy are described carefully as follows.

2.1 Fault Model

The PEs are essential building blocks and are connected regularly to construct a ME. Generally, PEs are surrounded by sets of ADDs and accumulators that determine how data flows through them. PEs can thus be considered the class of circuits called ILAs, whose testing assignment can be easily achieved by using the fault model, cell fault model (CFM) [21]. Using CFM has received considerable interest due to accelerated growth in the use of high-level synthesis, as well as the parallel increase in complexity and density of integration circuits (ICs). Using CFM makes the tests independent of the adopted synthesis tool and vendor library. Arithmetic modules, like ADDs (the primary element in a PE), due to their regularity, are designed in an extremely dense configuration. Moreover, a more comprehensive fault model, i.e. the stuck-at (SA) model, must be adopted to cover actual failures in the interconnect data bus between PEs [22].

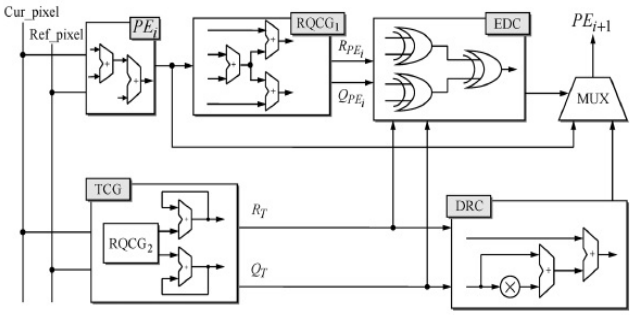

Figure 2: Specific EDDR testing proposed model

The SA fault is a well known structural fault model, which assumes that faults cause a line in the circuit to behave as if it were permanently at logic “0” (stuck-at 0 (SA0)) or logic “1” [stuck-at 1 (SA1)]. The SA fault in a ME architecture can incur errors in computing SAD values. A distorted computational error and the magnitude of are assumed here to be equal to, where denotes the computed SAD value with SA faults.

2.2 TCG Design

According to Fig. 2, TCG is an important component of the proposed EDDR architecture. Notably, TCG design is based on the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data. The specific in Fig. 2 estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macroblock. Thus, by utilizing PEs, SAD shown in as follows, N X Nin a macroblock with size of can be evaluated:

$$\text{SAD} = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}|xi - yj| = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}|(qxij * m + rxij) - (qxij * m + ryij)| \quad (1)$$

$$\text{Rt} = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}(xij - yij) \quad (2)$$

Fig. 4 shows the timing chart for a macroblock with a size of 4 X 4 in a specific to demonstrate the operations of the TCG

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circuit. The data and from Cur_pixel and Ref_pixel must be sent to a comparator in order to determine the luminance pixel value and at the 1st clock. Notably, if, then and are the luminance pixel value of Cur_pixel and Ref_pixel, respectively. Conversely, represents the luminance pixel value of Ref_pixel, and denotes the luminance pixel value of Cur_pixel when. At the 2nd clock, the values of and are generated and the corresponding RQ code, can be captured by the and circuits if the 3rd clock is triggered the 4th clock displays the operating results. The modulus value of is then obtained at the 5th clock. Next, the summation of quotient values and residue values of modulo are proceeded with from clocks 5–21 through the circuits of ACCs. Since a 4 X 4 macroblock in a specific of a ME contains 16 pixels, the corresponding RQ code (and) is exported to the EDC and DRC circuits in order to detect errors and recover data after 22 clocks. Based on the TCG circuit design shown in Fig. 4, the error detection and data recovery operations of a specific in a ME can be achieved.

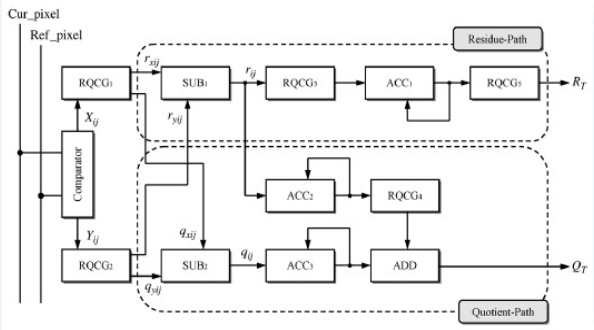

Figure 3: circuit design of the TCG

2.3 EDDR Processes

Fig. 2 clearly indicates that the operations of error detection in a specific are achieved by using EDC, which is utilized to compare the outputs between TCG and in order to determine whether errors have occurred. If the values of and/or, then the errors in a specific can be detected. The EDC output is then used to generate a 0/1 signal to indicate that the tested is error-free/errancy. This work presents a mathematical statement to verify the operations of error detection. Based on the definition of the fault model, the SAD value is influenced if either SA1 and/or SA0 errors have occurred in a specific. In other words, the SAD value is transformed to if an error occurred. Notably, the error signal is expressed as to comply with the definition of RQ code. Under the faulty case, the RQ code from of the TCG is thus, the error in a specific can be detected by the figure 4.

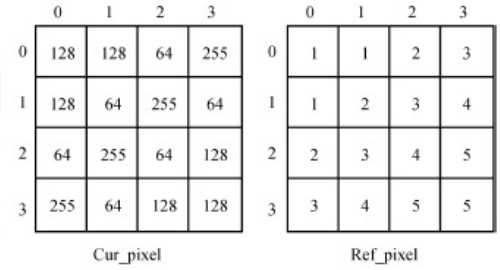

Figure 4: Example of pixel value

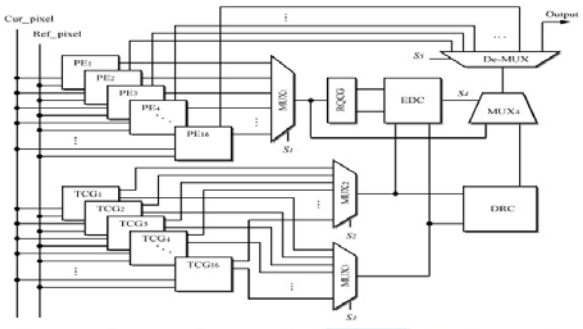

Figure 5: proposed EDDR architecture of the ME

To realize the operation of data recovery in (13), a Barrel shift [23] and a corrector circuits are necessary to achieve the functions of and, respectively. Notably, the proposed EDDR design executes the error detection and data recovery operations simultaneously. Additionally, error-free data from the tested or the data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific for subsequent testing.

2.4 Numerical Example

A numerical example of the 16 pixels for a 4 X 4 macroblock in a specific of a ME is described as follows. Fig. 5 presents an example of pixel values of the Cur_pixel and Ref_pixel. Based on (7), the SAD value of the 4 X 4 macroblock is:

$$\begin{aligned} \mathrm{SAD} &= m \times Q_T + R_T \\ &= (2^j - 1) \times Q_T + R_T \\ &= 2^j \times Q_T - Q_T + R_T. \end{aligned} \tag{3}$$

$$\begin{aligned} \mathrm{SAD} &= \sum_{i=0}^{3}\sum_{j=0}^{3} X_{ij} - Y_{ij} \\ &= |X_{00} - Y_{00}| + |X_{01} - Y_{01}| + \ldots + X_{33} - Y_{33} \\ &= (128 - 1) + (128 - 1) + \ldots + (128 - 5) \\ &= 2124. \end{aligned} \tag{4}$$

3. Result and Conclusion

This project proposes BISDC architecture for self detection and self-correction of errors of PEs in an MECA. Based on the error detection correction concepts of bi residue codes, this paper presents the corresponding definitions used in

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designing the BISD and BISC circuits to achieve self-detection and self correction operations. Extensive verification of the circuit design is performed using the VHDL and then synthesized by the Synopsys Design Compiler with TSMC 0.18- m 1P6M CMOS technology to demonstrate the feasibility of the proposed EDDR architecture design for ME testing applications. The time penalty is another criterion to verify the feasibility of the proposed EDDR architecture. Table I also summarizes the operating time evaluation of a specific and each component in the proposed EDDR architecture. The following equations show the time penalty of error detection and data recovery Performance evaluation reveals that the proposed BISDC architecture effectively achieves self-detection and self-correction capabilities with minimal area.

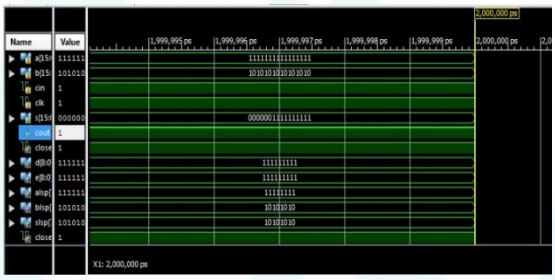

Figure 6: Explanation of the code adjustment

The Functional-simulation has been successfully carried out with the results matching with expected ones. The design functional verification and Synthesis is done by using Xilinx-ISE/XST and Cadence RTL Compiler of BISDC architecture for MECA. In this project the Area obtained is 87% using Cadence RTL Compiler.

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