Integrated Buck-Buck-Boost AC/DC Converter

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Abstract: Single-Stage transformerless AC/DC converter received much attention in the universal line application. Unlike the existing converters a new high step-down transformerless single-stage single-switch AC/DC converter is proposed. The topology integrates a buck-buck-boost converter with low intermediate bus and output voltage. The converter utilizes a buck converter as a PFC cell and buck-boost converter as a DC/DC cell. The buck-buck-boost converter is able to reduce the bus voltage below 150V under all input and output condition without using a step-down transformer. The absence of transformer reduces the component count, size and cost of the converter. Unlike the existing converter, buck-buck-boost is able to achieve simple control structure with single switch, positive output voltage and high power factor. By using DPT feature, converter is able to achieve high power conversion efficiency. The converter is successfully tested by using MATLAB/Simulink. The simulation result shows that the converter is a good tradeoff between reduced bus voltage and high power factor.

Keywords: Buck-buck-boost converter, power factor correction, single-stage single-switch, transformerless, Direct Power Transfer.

1. Introduction

With the widespread use of power electronics loads, more attention has been given to the power factor correction (PFC) and reducing harmonic distortion in the current drawn from the electric power utility. Moreover, with the stringent modern power quality standards [1], active PFC techniques have rapidly become a vigorous research topic in the power electronics field and considerable efforts have been made on the development of the PFC converters [2], [3].

Active PFC techniques are usually divided into two categories: two-stage and single-stage approaches. The two-stage approach can achieve good performance such as high power factor, low voltage stress and tight output voltage regulation [4]. The major drawbacks of the two-stage approach are its high cost, low power density, low conversion efficiency and complex control, particularly in low-power applications. To overcome these drawbacks, many single-stage PFC topologies have been recently proposed [5].

Single-Stage (SS) ac/dc converters have received much attention in the past decades because of its cost effectiveness, compact size and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [6]-[10]. Their intermediate bus voltage is usually greater than the input line voltage and easily goes beyond 450 V at high-line application. Therefore a bulky capacitor and high-voltage-rating semiconductors have to be used; this increases both the size and cost and will result in lower efficiency [11].

In an effort to reduce the dc voltage on the energy storage capacitor, a number of techniques have been introduced. However, most of the proposed techniques usually comprise of a boost converter for PFC followed by a DC-DC converter for output voltage regulation. With a simple step-down DC-DC cell (buck or buck-boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [12], [13].

A high step-down transformer is usually employed even when galvanic isolation is not mandatory. But leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14]-[16]. In [13], [18] and [19], the converters employ a buck-boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [19] and [13] process power at least twice resulting in low power efficiency. Moreover, the reported converters in [17] consist of two active switches leading to more complicated gate control.

The converter in [20] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. The converter operating with narrow duty cycle, this greatly increases the difficulty in its implementation due to the minimum on time of pulse-width-modulation (PWM) IC.

In this paper, a new power factor correction technology is proposed. The converter formed by two converters namely, a
buck converter as a PFC cell and a buck-boost converter as a DC-DC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. So a transformer is not needed to obtain the low output voltage.

Thus the converter is able to achieve:

1. Low intermediate bus and output voltages in the absence of transformer
2. Simple control structure with a single-switch
3. Positive output voltage
4. High conversion efficiency due to part of input power is processed once and
5. Input surge current protection because of series connection of input source and switch.

Buck-Buck-Boost (BuBuBo) converter circuit configuration and principle of operation is presented in Section II. Design consideration is illustrated in section III. Simulation result of buck-buck-boost converter is given in section IV. Finally conclusion is stated in section V.

2. Circuit Configuration and Principle

The Integrated BuBuBo converter which consists of a buck PFC cell (L1, S1, D1, C0 and Cb) and a buck-boost dc/dc cell (L2, S1, D2, D3, C0 and Cb) is illustrated in Figure 1 (a). Here L2 is on the return path of the buck PFC cell, it does not contribute to the cell electrically. Thus L2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L1 and L2 at the beginning of each switching cycle t0. Main advantages of DCM operation are:

1. Inherent PFC capability with zero-current switch turn ON
2. Reduction of the reverse recovery problem of the fast diodes in the circuit
3. Good and fast regulation of the output voltage
4. Low-cost power supply can be achieved because of its simplified control circuits

Due to the characteristic of buck PFC cell, there are two operating modes in this circuit. Buck converter operates only when input voltage is greater than output bus voltage.

Mode A (Buck-Boost Mode—V\textsubscript{in}(\theta) ≤ V\textsubscript{B} + V\textsubscript{0}): When the input voltage \( V\textsubscript{in}(\theta) \) is smaller than the sum of intermediate bus voltage \( V\textsubscript{B} \) and output Voltage \( V\textsubscript{0} \), the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage. Only the buck–boost dc/dc cell sustains all the output power to the load. So two dead-angles \((0 – \alpha)\)and \((\beta – \pi)\) are present in a half-line period and no input current is drawn as shown in Figure 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Figure 2 (a), (b) and (f). Figure 3(a) shows its current waveforms.

Mode B (Buck Mode—V\textsubscript{in}(\theta) > V\textsubscript{B} + V\textsubscript{0}): In this mode, when the input voltage is greater than the sum of intermediate bus voltage and output Voltage, buck PFC cell get activate. Buck converter operates in the conduction region in between \( \alpha \) and \( \beta \). The circuit operation over a switching period can be divided into four stages. The corresponding circuit is Figure 2(c), (d), (e) and (f). The waveforms are shown in Figure 3(b).

1. Stage 1 (d\textsubscript{T}1): Initially capacitor \( C\textsubscript{B} \) if fully charged. When switch \( S1 \) is turned ON, inductor \( L2 \) is charged linearly by the bus voltage \( V\textsubscript{B} \) in the capacitor \( C\textsubscript{B} \), while diode \( D2 \) is conducting. Thus the current flows from \( C\textsubscript{B} \), \( L2 \), \( S1 \) and D2 to \( C\textsubscript{B} \). Output capacitor \( C0 \) delivers power to the load.
2. Stage 2 (d\textsubscript{T}2): When switch \( S1 \) is turned OFF, diode \( D1 \) becomes forward biased and thus energy stored in inductor \( L2 \) is discharged through capacitor \( C0 \) and load \( R\textsubscript{L} \).
3. Stage 3 (d\textsubscript{T}3-d\textsubscript{T}4): The inductor current \( i\textsubscript{L2} \) is totally discharged through \( C0 \) & \( R\textsubscript{L} \) and \( C0 \) sustains the load current \( i\textsubscript{L0} \).
L₂ is released to C₀ and current is supplied the load through diode D₃. The stage ends once the inductor L₂ is fully discharged.

3. Stage 3(d₃Tₛ): Inductor L₁ continues to deliver current to C₀ and the load until its current reaches zero.

4. Stage 4(d₄Tₛ): Only C₀ delivers the output power to Rₗ.

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**Figure 2:** Circuit operation stages of the buck-buck-boost ac/dc converter

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**Figure 3:** (a) Key waveforms of buck-boost converter
(b) Key waveforms of buck converter

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### 3. Design Considerations

Some assumptions are taken to simplify the circuit analysis, they are:

1. All circuit components are ideal.
2. Input voltage $V_{in(\theta)} = V_{pk} \sin \theta$.
3. Both capacitors C₀ and C₀ are large so that both capacitors can be treated as constant DC voltage source without ripples.
4. Switching frequency Fₛ is much higher than input line frequency f.

Here filter capacitor and inductor are used to average the input current. Let consider resonance frequency Fᵣ as 2500Hz. Value of inductor and capacitor is calculated by the equation:
Depending on the application, the bulk capacitance value required could be dictated by voltage ripple requirement, hold-up requirements etc. The value of bus capacitance can be calculated from the relation:

\[ C_B = \frac{2 \times P_{out} \times t_{hold-up}}{V_{B-no-min}^2 - V_{B-min}^2} \]  

Where,

- \( P_{out} \) - Output power in Watt
- \( t_{hold-up} \) - Hold-up time
- \( V_{B-nominal} \) - Nominal bus voltage calculated by iteration
- \( V_{B-min} \) - Minimum permissible bus voltage (± 6%)

Here both cells operating in DCM mode throughout the ac line period. Thus it must determine critical values of \( L_1 \) and \( L_2 \) such that, both cells operates in DCM when the inductor values are less than their critical values. The critical inductances are calculated by using the relation:

\[ L_{1-crit} = \frac{R_{L-min} T V_{pk} d_{1-max}}{2 \pi \times V_0^2} \left[ V_{pk} \left( \frac{A}{2} + \frac{V_T}{4} \right) + V_T \times B \right] \]

\[ L_{2-crit} = \frac{R_{L-min} V_B^2 T_s}{2V_0^2} d_{1-max} \]

Where,

\[ V_T = V_B + V_0 \]  
\[ A = \sin 2\alpha - \sin 2\beta \]  
\[ B = \cos \alpha - \cos \beta \]  
\[ d_{1-max} = \begin{cases} \min(d_{1-DC}, d_{1-DC/DC}), & \alpha < \theta < \beta \\ d_{1-DC/DC}, & \text{otherwise} \end{cases} \]

Let \( R_{L-min} = 100\Omega \)  
\( V_0 = 80V \)

The output filter capacitance should be selected in order to reduce the ripples presented in the output voltage. The value of capacitance is calculated by using the relation:

\[ C_0 = \frac{1}{4\pi f f} \left[ 1 + \frac{1}{\sqrt{2Ripplefactor}} \right] \]

| Input Voltage | 230V rms |
| Output Voltage | 80V |
| Filter Inductance | 2mH |
| Filter Capacitance | 2µF |
| Inductance \( L_1 \) | 106µH |
| Inductance \( L_2 \) | 30µH |
| Bus capacitance \( C_B \) | 5mF |
| Output capacitance \( C_0 \) | 5mF |
| Load resistance \( R_L \) | 100Ω |
| Switching frequency | 20kHz |
| Switch type | MOSFET |

4. Simulation Results

Simulation circuit for a buck-buck-boost converter with input voltage 230V rms and output voltage of 80V DC is shown in Figure 4. The circuit components are selected in accordance to the relation (1)-(9) and are listed in the table 1.

Figure 4: Simulation model of buck-buck-boost converter

Figure 5: Simulation model of PFC block
5. Conclusion

The Integrated Buck-Buck-Boost single-stage AC/DC converter has been verified experimentally by using MATLAB/Simulink. Buck-Buck-Boost converter is very useful for all universal line application. By using this converter, it is able to achieve bus voltage below 150V at all input and output conditions. So the converter can able to achieve less bus voltage and output voltage without using any resonant converters, high step transformers etc. Thus unlike all the existing converters, Buck-Buck-Boost converters can reduce the component count and complexity in control. Reduced bus voltage allows using low voltage intermediate capacitor. By using Buck-Buck-Boost converter, it is able to achieve a power factor around 0.97. Thus the converter can meet IEC 61000-3-2 standard.

References


Author Profile

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