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# Static Power Reduction of a Pulse Enhanced Flip Flop

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**Abstract:** ***Flip Flops form an important component of most digital systems today. Flip flops act as the memory elements for many memory chips and microprocessors. Pulse enhancement of the flip flops is done in order to improve their performance and increase the speed. Flip-flop is one of the components of digital systems that consume most of the power due to the presence of clock. As the power budget of today's portable digital circuit is severely limited. Thus consumption of power needs to be minimized. The major factor contributing in the power consumption is the static power. The situation which has cropped up has made it necessary to devise methods to reduce the static power of a flip flop. This paper presents some methods application of which is expected to significantly reduce the static power. A tradeoff between power and area is required here.***

**Keywords:** Pulse enhancement, Static Power, Trade off

## 1. Introduction

Static power is the power consumed while there is no circuit activity. Static power dissipation is mainly due to sub threshold conduction through OFF transistors, tunneling current through gate oxide and leakage through reverse-biased diodes. Below 130nm static power is rapidly becoming a primary design issue eventually; static power dissipation may become comparable to dynamic power. Both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current (called sub threshold current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages ($V_{dd}$ might have been 5 V and $V_{th}$ for both NMOS and PMOS might have been 700 mV). $SiO_2$ is a very good insulator, but at very small thickness levels electrons can tunnel across the very thin insulation; the probability drops off exponentially with oxide thickness. Tunneling current becomes very important for transistors below 130 nm technology with gate oxides of 20 Å or thinner. This is one of the reasons of static power dissipation. Another reason is leakage through reverse biased diodes. Small reverse leakage currents are formed due to formation of reverse bias between diffusion regions and wells (for e.g., p-type diffusion vs. n-well), wells and substrate (for e.g., n-well vs. p-substrate). In modern process diode leakage is very small compared to sub threshold and tunneling currents, so these may be neglected during power calculations. Power dissipation is unavoidable especially as technology scales down. Techniques must be devised to reduce power dissipation. The following section describes some approaches to reduce the static power to some extent. These are then applied to flip flop in consideration and the power dissipated is then compared for each case.

### A. Sleep Transistor Technique

The concept of the sleep transistor is straight forward. A sleep transistor is either a pMOS or nMOS high VT transistor and is used as a switch to shut off power supplies to parts of a design in standby mode. The pMOS sleep transistor is used to switch VDD supply and hence is called a "header switch." The nMOS sleep transistor controls VSS supply and hence is called a "footer switch." In designs at and below, either a header or footer switch is used due to tight voltage margin and too large area penalty when both header and footer switches are implemented. The sleep transistor approach with both header and footer transistors is shown in the fig.1.

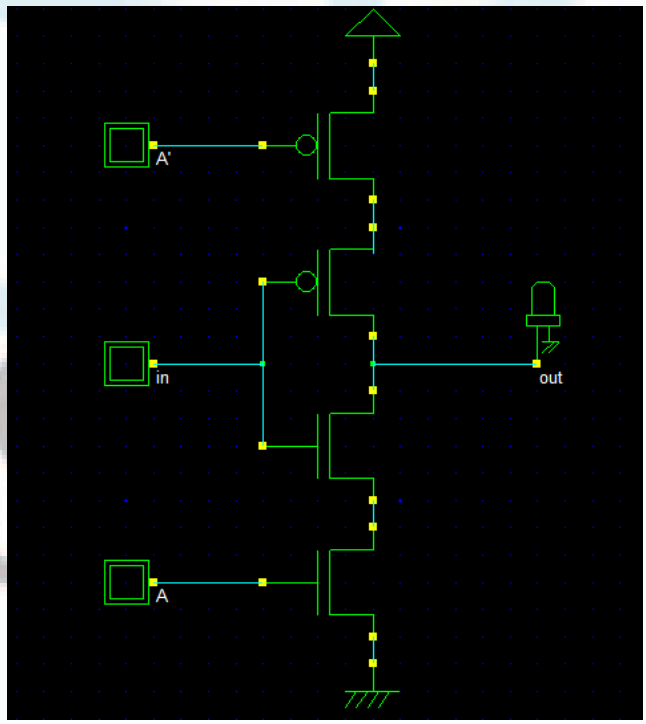


**Figure 1:** Sleep Transistor Technique

### B. Sleepy Stack Technique

It is a state-saving ultra low-leakage technique and is a combination of the sleep transistor and forced stack technique. The sleepy stack technique is shown in fig.2.

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From the figure, during active mode, sleep transistors are on then reduced resistance increases current while reducing delay. During sleep mode, sleep transistors are off; stacked transistors suppress leakage current while saving state.

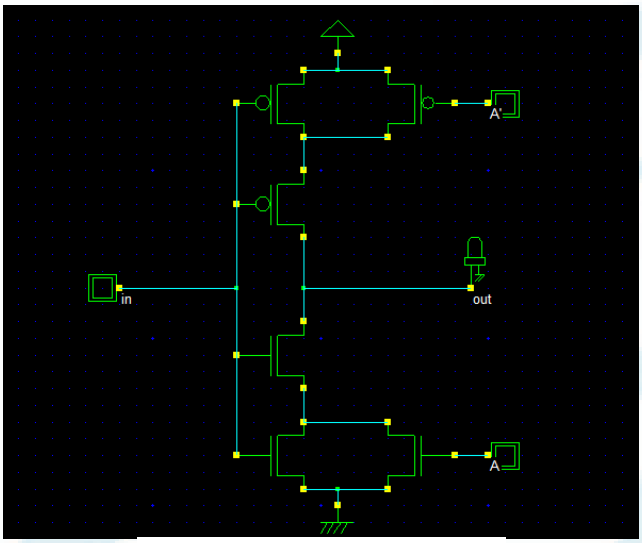


**Figure 2:** Sleepy Stack Technique

### C. Sleepy Keeper Technique

Sleepy keeper uses traditional sleep transistors plus two additional transistors - driven by a gate's already calculated output - to save state during sleep mode. It reduces leakage current while saving exact logic state. Like the sleepy stack approach, sleepy keeper achieves leakage power reduction equivalent to the sleep approach but with the advantage of maintaining exact logic state (instead of destroying the logic state when sleep mode is entered). Sleepy keeper structure is obtained by adding sleep transistors and two transistors driven by output viz. NMOS to pull-up network, PMOS to pull-down network. During active mode, sleep transistors are on thus reducing delay and during sleep mode, sleep transistors are off thus saving state. It offers less area penalty and faster than sleepy stack approach. (fig.3.)

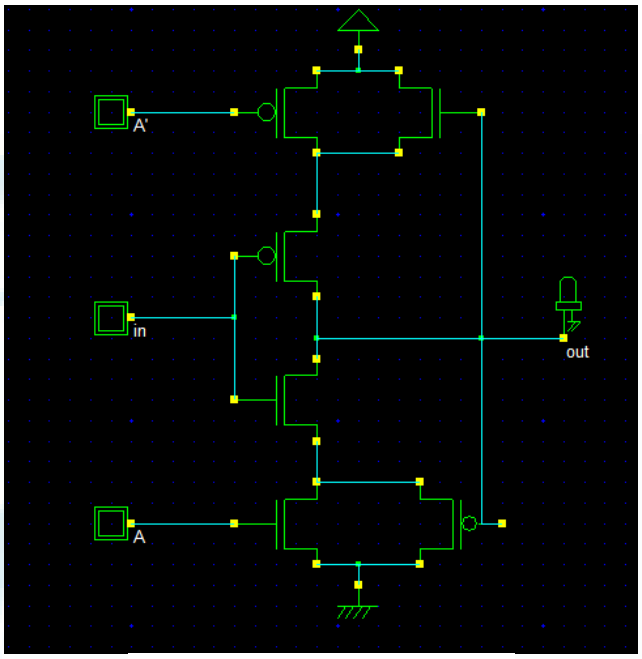


**Figure 3:** Sleepy Keeper Technique

### D. Dual Sleep Technique

Dual sleep method reduces leakage current and saves area in a considerable amount. It also saves exact logic state which makes it better than traditional sleep approach. Area requirement is maximum for this technique since every transistor is replaced by three transistors. Dual sleep Technique includes two extra pull- up & pull-down transistors in sleep mode either in OFF/ON state (fig.4.).

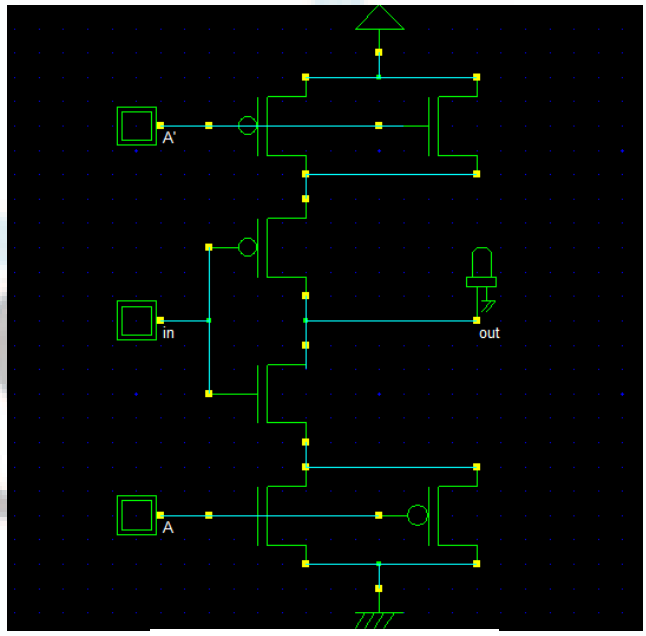


**Figure 4:** Dual Sleep Technique

### E. Dual Stack Technique

The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power

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product. Especially it shows nearly 50-60% of power than the existing normal or conventional future integrated circuits for power & area efficiency flip-flops. So, it can be used for. Fig.5. shows the dual stack approach with two PMOS transistors in pull down network and two NMOS transistors in pull up network.

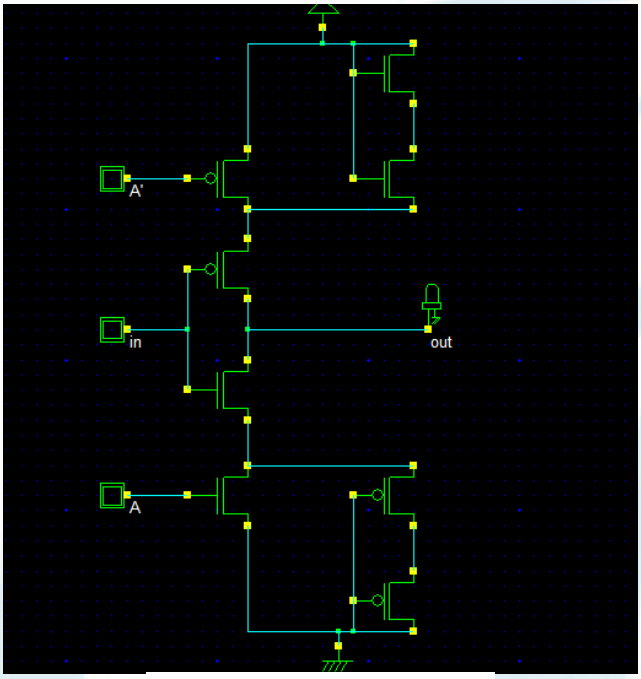


**Figure 5:** Dual Stack Technique

## 2. Pulse Enhanced Flip Flop

Flip Flops are synchronous bistable devices. The term synchronous means the output changes state only when the clock input is triggered. That is, changes in the output occur in synchronization with the clock. The term pulse triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. As this kind of flip-flops are sensitive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up prior to the clock pulse's rising edge and must not be changed before the falling edge. Otherwise, ambiguous results will happen. It is estimated that the power consumption of the clock system, which consists of the clock distribution networks and storage elements is as high as 20% to 45% of the total system power. It is beneficial to lowering the power consumption of the clock tree system. The conventional flip flops are very sensitive to clock skew and jitter. Flip are the basic storage elements used extensively in all kinds of digital designs. Lowering of the power consumption thus becomes an important issue of concern in order to improve the performance of the digital systems. The technique of pulse enhancement was introduced and applied on the pulse triggered flip flop in order to achieve this. A pulse triggered flip flop with pulse enhancement scheme is shown in the figure below.

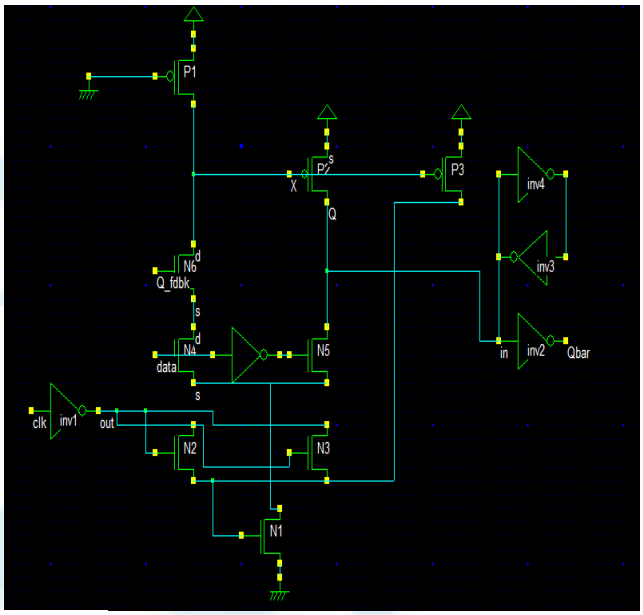


**Figure 6:** Schematic of P-FF design with pulse enhancement scheme

A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered Flip Flop. The circuit complexity of a P-FF is simplified since only one latch as opposed to two used in conventional master slave configuration , is needed , P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time . P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network.

**Table 1:** Power of P-FF

| *Power* | *Setup Time* | *Hold Time* |
|---|---|---|
| 1.326e-5 | -5.002e-10 | 1.500e-9 |

These parameters can be further improved by using the different 5 techniques mentioned in the first section. This would lead to further reduction in power which would make the design more power efficient. However this technique is mostly applicable in places where reduction in power is of prime importance and slight compromise in terms of area is not a matter of concern. Thus a tradeoff between power and area has to be considered.

## 3. Reduction in Power

The major concern here is the reduction in static power of P-FF. The purpose can be solved by incorporating the various techniques mentioned in the above section. The technique mainly consists in adding the various configurations of the transistors explained in section I to the P-FF structure in the same way as they are added in the inverter configuration .After this has been done the power, set up time and hold time are again calculated using HSPICE as done in the power calculation of the P-FF. HSPICE is an analog circuit

simulator capable of performing transient, steady state, and frequency domain analyses. It can be used to simulate electrical circuits in steady-state, transient, and frequency domains. Thus the power is calculated and tabulated as follows for each of the technique.

**Table 2:** Power Comparison

| | *Power* | *Setup Time* | *Hold Time* |
|---|---|---|---|
| Sleep | 9.427e-6 | -5.002e-10 | 1.005e-9 |
| Sleepy Stack | 7.138e-6 | -5.002e-10 | 1.005e-9 |
| Sleepy Keeper | 5.503e-6 | -5.002e-10 | 1.005e-9 |
| Dual Sleep | 8.504e-6 | -5.002e-10 | 1.005e-9 |
| Dual Stack | 1.823e-6 | -5.002e-10 | 1.005e-9 |

The above table lists the power dissipated by P-FF in case of different configurations used. We find that the power is lower than the original circuit design in each case however the dual stack technique gives lowest power dissipation. But at the same time requires largest number of transistors as compared to the other techniques. Thus in places where the reduction in power plays a major role and the increase in area can be compromised for, dual stack technique is the best one can use. All these power calculations are carried out using 90nm technology

## 4. Conclusion

The paper aims at further reducing the static power consumption of the pulse enhanced edge triggered flip flop. The techniques used to carry out this are listed in section I. After carrying out the power calculation for each technique involved using HSPICE in 90nm technology we conclude that the dual stack technique reduces the power dissipation to the largest extent. Since the sole aim of the paper is to decrease the static power of the flip flop, the increase in area as a result of the increase in number of transistors is not accounted for nd is the matter of further research.

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