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Ground Bounce Noise Reduction Using Power Gating Techniques

Lekshmi Vijayan[1], Sukanya Sundaresh[2]

[1]PG Scholar, Dept. of Electronics and Communication Engg, TKM Institute of Technology, Kollam, Kerala, India
[2]Asst.Professor, Dept. of Electronics and Communication Engg, TKM Institute of Technology, Kollam, Kerala, India

Abstract: ***Any computational circuit is incomplete without an adder. The adder cells commonly consume less power and offers high speed. There are several techniques to reduce leakage power and ground bounce noise. This work makes use of power gating techniques in CMOS technology to reduce leakage power and ground bounce noise in mobile applications. It can be mainly divided into two types such as fine-grained power gating and coarse-grained power gating. In fine-grained power gating area consumption is increased due to large number of sleep transistors. In this project coarse-grained power gating technique is used to overcome this problem. In this design, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. A sleep transistor is referred to either a high threshold voltage pMOS or nMOS transistors. The sizing of transistors plays a key role in the static CMOS style. Here the conventional CMOS 28 transistor adder is considered as base case. This work also aims to design an ALU circuit using power gating technique. The ground bounce noise and leakage power are analyzed for a conventional CMOS full adder and an ALU circuit. The major performance criteria considered in this design are standby leakage power, ground bounce noise, and area. The simulations are performed by using DSCH2 and MICROWIND2 with different CMOS technologies.***

Keywords: Sleep Transistor, Power Gating, Ground Bounce Noise

1. Introduction

In recent years the demand for low power devices has been increases tremendously. Low power consumption, speed of the system and the small area are the three main factors for increasing the performance. Reducing power dissipation is one of the most important issue in very large scale integration design today. As technology scales into the nanometer regime ground bounce noise and noise immunity are becoming important metric of comparable importance to leakage current, active power and area for the analysis and design of complex arithmetic logic circuits. Static power consumption is a major concern in nanometer technologies. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. Reduction in leakage power has become an important concern in low-voltage, low power, and high performance applications. This demand may be due to fast growth of battery operated portable applications such as cell phones, laptops and other handheld devices. There are three major components of power dissipation in complementary metal oxide circuits such as switching power, short circuit power and static power [8]. Reducing any of these components will end up with low power consumption of the whole work.

For the design and analysis of complex arithmetic circuits, ground bounce noise is given an equal importance in the list of low power performance measuring parameters like leakage power, active power, ground bounce noise and area.
Noise immunity has been carefully considered since the significant threshold current of the low threshold voltage transition becomes more susceptible to noise. So here a new transistor resizing approach for 1bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power and ground bounce noise was introduced [1]. Power gating is a commonly used low-power design technique that is very effective in reducing power of a circuit during standby. To improve the peak of ground bounce noise staggered phase damping technique is also used [2].

In this work "Comparison and Application of different Power Gating Techniques in Circuits using CMOS" a conventional CMOS 28 transistor full adder is considered as the base case. The CMOS structure combines pMOS pull up and nMOS pull down networks to produce considered outputs. One of the most significant advantages of this full adder was its high noise margins and thus reliable operation at low voltages. The layout of CMOS gates was also simplified using the complementary transistor pairs. Over the past two decades, CMOS technology has played important role in designing high performance systems because of the advantages that CMOS provides: an exceptionally low power-delay-product, the ability to accommodate millions of devices on a single chip. To take the benefits of CMOS technology an Arithmetic and Logic Unit circuit is also proposed in this work. The ALU is a combination circuit that performs a number of arithmetic and logical operations [13]. To reduce leakage power, several techniques have been proposed in the CMOS full adder and the ALU circuits. Power gating is one such well known technique to reduce the leakage power [4] & [5].

2. System Architecture

Low power consumption, speed of the system and the small area are the three main factors for increasing the performance of a circuit. Delay and power dissipation of a circuit have also emerged as major concerns of designers and depend on the number of transistors used in the circuit. The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power dissipation [6] & [7]. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode. One of the most promising mechanisms for reducing leakage energy is power gating, whereby leakage energy is saved by cutting the supply voltage to idle circuits. Power gating is a power-saving technique; the supply voltage

is turned off during the standby mode by using a pMOS transistor or an nMOS transistor [4]. In the active mode, the sleep transistor is turned on to retain the functionality of the circuit. In the sleep mode, the sleep transistor is turned off, and thus cutting off the leakage path.

Moreover, new technologies with smaller feature sizes and lower supply voltages contribute to lowering power dissipation. In this project CMOS full adder and ALU circuits are used to explain the concept of reducing power consumption, which also explains the advantages of CMOS implementation and various design techniques used to make it more efficient [13]. Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems. The design of a full adder having low-power consumption results of great interest for the implementation of modern digital systems. ALU is the main part of the processor, designed using CMOS because it uses various flexible design techniques to reduce delay, chip area, power, and cost and to increase speed. Also, CMOS approach helps in accommodating large number of transistors on a single chip. All these improve the performance of the ALU and overall improve the performance of the system. In this project an eight functions instruction set for CMOS ALU that performs functions like AND, NAND, OR, NOR, XOR, XNOR, Addition and Subtraction.

A. Power Consumption in CMOS VLSI Circuits

The most important performance parameters for VLSI systems are speed and power consumption. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously. There are three major components of power dissipation in CMOS circuits: switching power, short circuit power and static power [8]. Reducing any of these components will end up with low power consumption of the whole system. The first two components are referred to as dynamic power. Dynamic power accounts for the majority of the total power consumption in digital CMOS VLSI circuits. The current pulse from VDD to GND results in a short circuit dissipation. Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. The total power is given by the following equation

$$P_{total}=V_{dd}^2.F_{clk}.C_{load}+V_{dd}.\sum_i I_{isc}+V_{dd}.I_l \ldots\ldots(1)$$

Where V_{dd} is the power supply voltage, F_{clk} is the system clock frequency, C_{load} is the load capacitance , $I_{i\,sc}$ is the short-circuit current at node I and I_l is the leakage current.

Static power is also known as idle power or leakage power. To understand how leakage current arises, one must understand how transistors work. A transistor regulates the flow of current between two terminals called the source and the drain. Between these two terminals is an insulator, called the channel that resists current. As the voltage at a third terminal, the gate, is increased, electrical charge accumulates in the channel, reducing the channel's resistance and creating a path along which electricity can flow. Once the gate voltage is high then it allows the normal flow of current between the source and the drain. The threshold at which the gate's voltage is high enough for the path to open is called the threshold voltage. As the equation that follows illustrates, leakage power consumption is the product of the supply voltage (V) and leakage current (I_{leak}), or parasitic current, that flows through transistors even when the transistors are turned off.

$$P_{leak} = V\, I_{leak} \ldots\ldots(2)$$

B. Conventional CMOS logic style

Conventional CMOS Logic is a type of static logic style. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. CMOS circuits are constructed in such a way that all pMOS transistors must have either an input from the voltage source or from another pMOS transistor. Similarly, all nMOS transistors must have either an input from ground or from another nMOS transistor. The composition of a pMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an nMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET to not conduct while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption.

In short, the outputs of the pMOS and nMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behavior of input and output, the CMOS circuits' output is the inverse of the input. The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and GND depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. An important characteristic of a CMOS circuit is the duality that exists between its pMOS transistors and nMOS transistors. A CMOS circuit is created to allow a path always to exist from the output to either the power source or ground. To accomplish this, the set of all paths to the voltage source must be the complement of the set of all paths to ground. This can be easily accomplished by defining one in terms of the NOT of the other. Due to the De Morgan's laws based logic, the pMOS transistors in parallel have corresponding nMOS transistors in series while the pMOS transistors in series have corresponding nMOS transistors in parallel.

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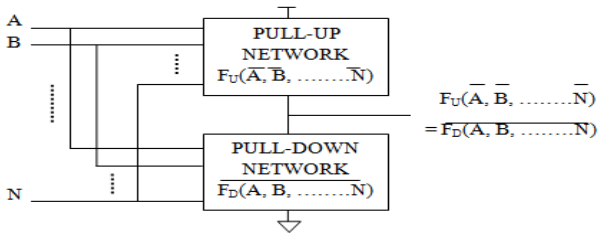

Figure 1: Conventional CMOS principle

An advantage of CMOS over nMOS is that both low-to-high and high-to-low output transitions are fast since the pull-up transistors have low resistance when switched on, unlike the load resistors in nMOS logic. CMOS logic dissipates less power than nMOS logic circuits because CMOS dissipates power only when switching. In addition, the output signal swings the full voltage between the low and high rails. This strong, more nearly symmetric response also makes CMOS more resistant to noise. Conventional CMOS devices work over a range of−55 °C to +125 °C and presents robustness against voltage scaling and high noise margins, so allowing a reliable operation at low voltages. Other advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and arbitrary transistor sizes. Input signals are connected to transistor gates only, which facilitates the usage and characterization of logic cells. The layout of CMOS gates is straightforward and efficient due to the complementary transistor pairs. Basically, CMOS fulfils all the requirements regarding the ease-of-use of logic gates.

C. Ground bounce noise

Ground bounce defines a condition when a device's output switches from high to low and causes a voltage change on other pins. It is usually seen on high density VLSI where insufficient precautions have been taken to supply a logic gate with a sufficiently low resistance connection to ground. Ground bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die. Essentially it is caused by a current surge passing through the lead inductance of the package. The problem is cause by the large current flow through the ground pin which develops a voltage drop over the lead inductance. This voltage drop on the ground line creates two main problems: first it raises the chip off ground potential which in turn increases the devices input threshold level, and secondly increases the voltage level on an output pin which is not switching. This is also called Simultaneous Switching Noise [2].

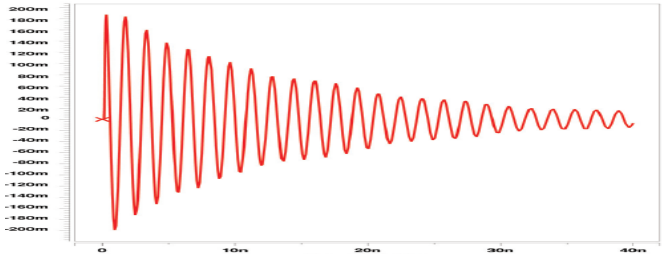

Figure 2: Ground bounce noise

Fig. 2 shows the graphical representation of ground bounce noise. In this phenomenon, when the gate is turned on, enough current flows through the emitter-collector circuit that the silicon in the immediate vicinity of the emitter is pulled high, sometimes by several volts, thus raising the local ground, as perceived by the transistor, to a value significantly above true ground. Relative to this local ground, the base voltage can go negative, thus shutting off the transistor. Otherwise it is the large sudden current that flows through the power and ground rails during standby-to-active mode transition. This results in long period of power and ground rails' fluctuation, due to the inductance of the off-chip packaging and the on-chip power grids. This resonance noise sometimes referred to as ground bounce noise or simultaneous switching noise [3]. This noise occurs in both power networks during mode transition, and the fluctuation in the power network.

D. Circuit design

D.1 Conventional CMOS 28T full adder design

The 28 Transistor full adders is the pioneer CMOS traditional adder circuit. This is considered as a base case throughout this project. All comparisons are done with this base case. Conventional CMOS implementation consists of two functional blocks pull-up and pull-down. Pull-up functional block is implemented with p-channel MOS transistors and pull-down functional block is implemented with n-channel MOS transistors. It is observed in the conventional adder circuit that the transistor ratio of pMOS to nMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters.

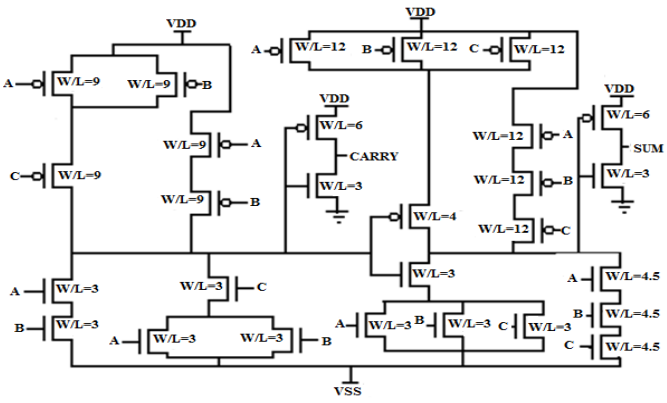

Figure 3: Conventional CMOS full adder

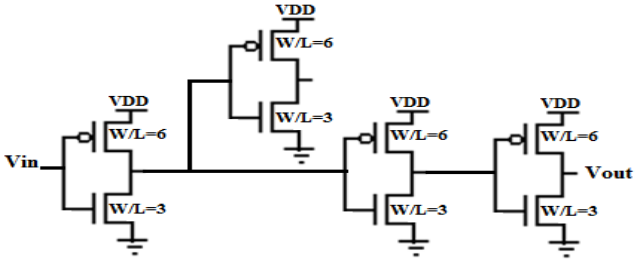

Figure 4: Equivalent circuit for conventional CMOS full adder

Fig. 3 shows the conventional CMOS 28 transistor adder [3]. The first 12 transistors of the circuit produce the CARRY and the remaining transistors produce the SUM outputs.

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Therefore the delay for computing CARRY is added to the total propagation delay of the SUM output. Base case is considered as individual block as shown in Fig. 4. Each block has been treated as an equivalent inverter. The same inverter ratio is maintained on each block. These sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the W/L ratio of transistor. The MOS transistor's performance varies with its channel length and channel width. On the other hand, these reduced sizes will reduce the area occupied by the circuit. This will reduce the silicon chip area and obviously there will be a reduction in the cost.

D.2 ALU design

The ALU is the core of a CPU in a computer. In this project an eight function instruction set for CMOS ALU that performs functions like AND, OR, NAND, NOR, XOR, XNOR, Addition and Subtraction. The input and output sections consist of a 8 to 1 multiplexer. Each of these functions is performed on three 1- bit input operations and results a single bit ALU [13]. Fig. 5 shows the functional block diagram of an ALU.

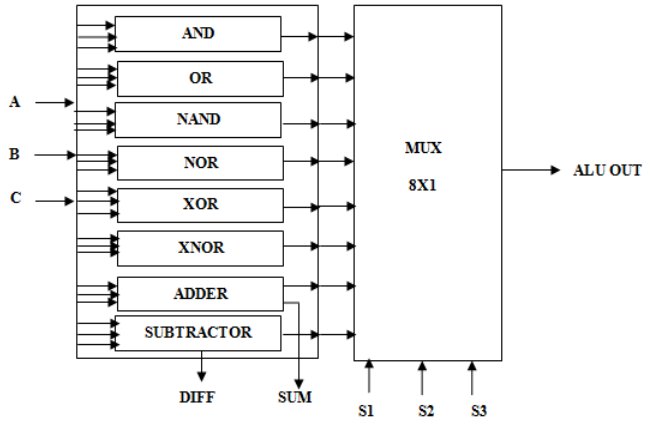

Figure 5: Functional block diagram of ALU

E. Leakage reduction techniques

E.1 Power gating technique

There are several VLSI techniques to reduce leakage power. Power gating is one of the most effective methods recently developed [4] & [5] to reduce power in the standby mode. In a power gating design, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. A sleep transistor is referred to either a high threshold voltage pMOS or nMOS transistors which are used as switches to disconnect power supplies from design modules during standby mode. In active mode, the sleep transistor is on and the circuit functions as usual. In standby mode, the switch transistor is turned off, which disconnects the logic gate from power or ground.

Fig. 6 shows a power gated block using footer and header switch. The nMOS sleep transistor controls VSS supply and hence is called footer switch. In this power gating technique the source nodes of the gates in the functional block which were grounded are connected to the drain of the nMOS sleep transistor. The pMOS sleep transistor is used to switch VDD supply and hence is named header switch.

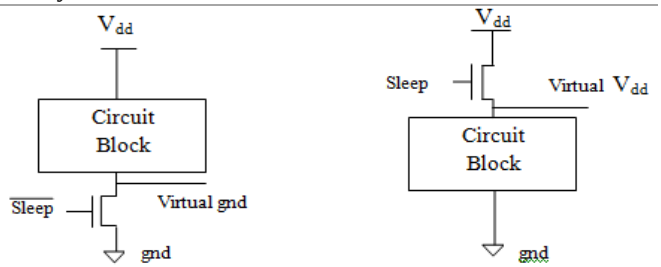

Figure 6: Power gating with footer and header switch

The application of sleep transistors for power gating is one of the most effective methods to reduce standby leakage. Thereby, the sleep transistors create a virtual power and/or a virtual ground. That means in theory, during standby all leakage currents of the gated module are zeroed. It should be noted that even when all sleep transistors are switched off a small leakage component exists. This is mainly based on sub-threshold leakage of the sleep transistors. Footers are generally more area efficient as the high n-type mobility means less of them are needed. That being said, most commercial designs implement headers due to easier design and analysis.

Power gating can be mainly divided into two types such as fine-grained power gating and coarse-grained power gating. If the power-gated cells in a standard cell design are used in an isolated manner, i.e., their virtual VDDs are not connected, we call this power gating approach fine-grained power gating. Adding a sleep transistor to every cell that is to be turned off imposes a large area penalty, and individually gating the power of every cluster of cells creates timing issues introduced by inter cluster voltage variation that are difficult to resolve. Fine-grained power gating encapsulates the switching transistor as a part of the standard cell logic. If a sleep transistor is shared by a cluster of power-gated logic cells such kind of power gating is called coarse-grained or cluster-based power gating, i.e., their virtual VDDs are connected together. The coarse-grained approach implement the grid style sleep transistors which drives cells locally through shared virtual power networks. In coarse-grained power gating, the power-gating transistor is a part of the power distribution network rather than the standard cell.

E.2 Staggered-phase damping technique

During the power mode transition, an instantaneous charge current passes through the sleep transistor, which is operating in its saturation region, and creates current surges elsewhere. Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these surges result in voltage fluctuations in the power rails. If the magnitude of the voltage surge or circuit may erroneously latch to the wrong value or switch at the wrong time. Inductive noise, also known as simultaneous switching noise, is phenomenon that has been traditionally associated with input/output buffers and internal circuitry. The noise immunity of a circuit decreases as its supply voltage is reduced such as power gating to address the problem of ground bounce in low-voltage CMOS circuits [2]. The staggered-phase damping technique is described considering a CMOS full adder power domain of two clusters shown in Fig. 7.

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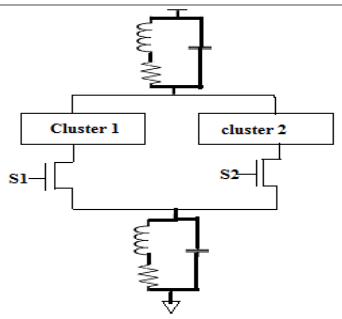

Figure 7: Staggered phase damping technique

When a power domain is turned on while other power domains located at proximity to that power domain are active, these power and ground fluctuations reduce the noise margin of the active circuits, which can result in functional errors. This is a critical problem, especially for low supply voltage design where the added power and ground noise can be a significant portion of the total voltage swing. During standby-to-active power mode transition, the proposed staggered-phase damping delays the activation time of one of the two sleep transistors relative to the activation time of the other one by a time that is equal to half the resonant oscillation period that can be determined through simulation or from the LC values. As a result, noise cancellation occurs once the second sleep transistor turns on due to the phase shift between the noise induced by the first sleep transistor and that induced by the second sleep transistor. An initial spike occurs once the first sleep transistor turns on followed by noise cancellation once the second sleep transistor turns on. The initial spike determines the peak noise, thus the proposed technique is not very effective in reducing the peak noise due to this initial spike. However, the proposed technique is very effective in reducing the settling time due to the noise cancelation that suppresses the fluctuations once the second sleep transistor turns on.

3. Simulation Results

Circuit simulations are done by using DSCH2. Fig. 8 and Fig. 9 shows the simulation result of a conventional CMOS full adder and ALU.

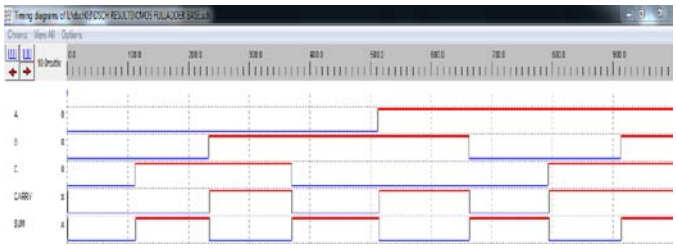

Figure 8: Waveform of conventional CMOS full adder in DSCH2

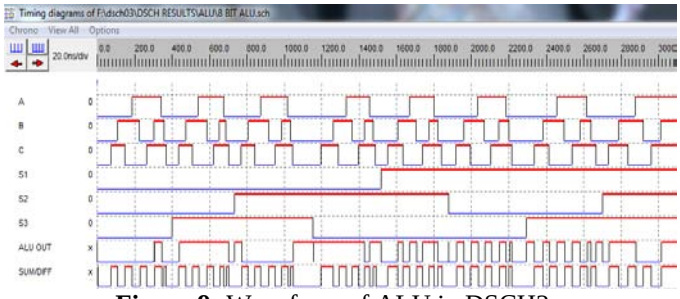

Figure 9: Waveform of ALU in DSCH2

A. Active Power

The power dissipated by the circuit when the circuit is in active state. Considered simulation time to calculate active power is 10ns for CMOS full adder and 100ns for ALU. Input vectors have been given in such a way that it covers almost all input vector combinations. The same vectors and simulation time has been given to base case to compare the results with different CMOS technologies and the result is shown in Table.1.

B. Area

The layouts are used to calculate the areas of proposed designs [9]. Layouts of proposed full adder circuit and ALU are shown in Fig. 10 and Fig.12 and the simulation results are shown in Fig. 11 and Fig.13. Along with technology scaling down the area of the CMOS full adder and the ALU circuits are reduced and the result is shown in Table.1.

Table 1: Power & Area comparison with different CMOS technologies

CMOS Technology	CMOS Full Adder		ALU	
	Power	Area	Power	Area
350nm	0.772mW	7069.9μm^2	4.347mW	77176.3μm^2
250nm	0.205mW	2761.7μm^2	1.394mW	30147.0μm^2
180nm	96.207μW	1767.5μm^2	0.659mW	19294.1μm^2
120nm	9.662μW	407.4μm^2	0.112mW	8799.1μm^2
90nm	9.488μW	358.6μm^2	97.166μW	8540.7μm^2
70nm	4.386μW	332.4μm^2	35.777μW	5811.9μm^2

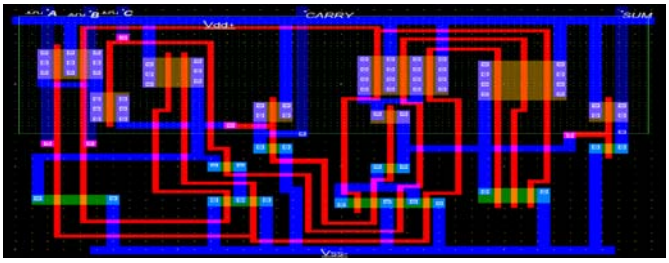

Figure 10: Layout of CMOS Full adder

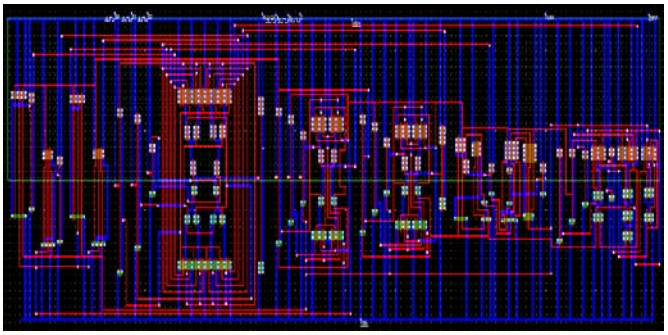

Figure 11: Layout of ALU

The proposed work consists of the comparison of different power gating techniques such as coarse-grained power gating with footer and header switches and fine-grained power gating with footer and header switches. Also for improving the peak of the ground bounce noise reduction staggered-phase damping technique is used.

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Table 2:. Comparison of different power gating techniques

Circuits	Power Switch	CMOS Full adder	ALU
Base Case	———	9.488µW	45.389µW
Fine Grained Power Gating	Footer Switch	7.754µW	5.088µW
	Header Switch	6.487µW	3.553µW
Coarse Grained Power Gating	Footer Switch	5.028µW	5.082µW
	Header Switch	3.014µW	3.936µW
Staggered Phase Damping Technique	———	0.868µW	———

C. Ground Bounce Noise Reduction

Power gating is an effective method to reduce leakage power during the circuit in sleep mode; it introduces the ground bounce problem and has considerable energy consumption during the mode transitions. In this work, low leakage 1 bit full adder cell and an ALU circuit is proposed for low ground bounce noise. Here the peak amplitude of ground bounce noise is reduced by using power gating techniques and the result is shown in Fig.12 and Fig.13.

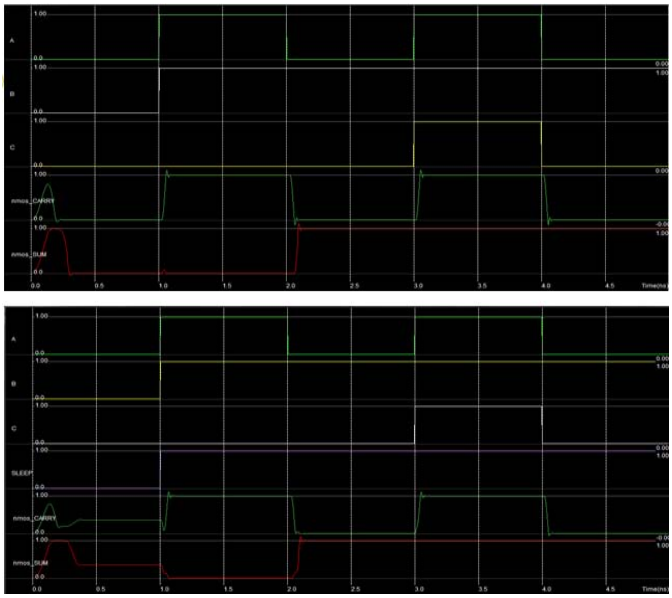

Figure 12: Noise reduction in CMOS full adder

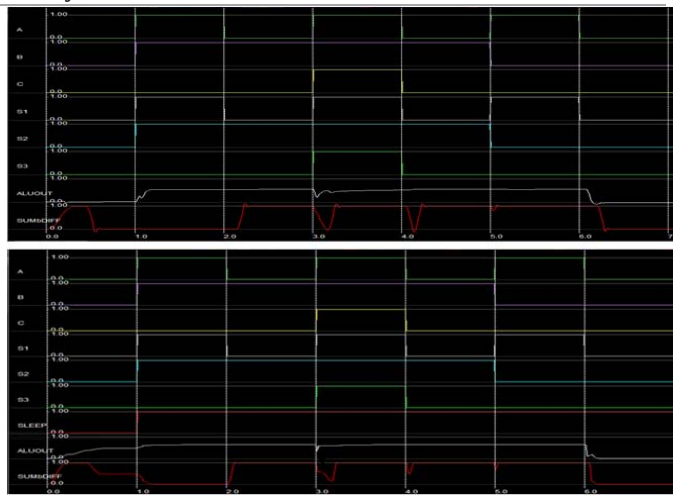

Figure 13: Noise reduction in ALU

4. Conclusion

Low power consumption is targeted at the circuit design level. This project intends to reduce the ground bounce noise caused by large discharge current through a sleep transistor during the mode transition of the power gating structure. Here different power gating structures are proposed to reduce the magnitude of voltage glitches in the power distribution network. In this work, low leakage 1 bit full adder cell and an ALU circuit is proposed for low ground bounce noise. Logic design and circuit design of conventional CMOS full adder and an ALU having eight functions are completed and also verified the simulation results. Also the power and area comparison is done by using the automatically generated layouts. After applying power gating technique active power is reduced by 19% in comparison to CMOS full adder and 89% in comparison to ALU. Hence the noise immunity of proposed circuits are also reduced. For calculating the area layout design of CMOS full adder and ALU were done. The proposed 1-bit full adder and an ALU are performed by using DSCH2 and Microwind2 with different CMOS technologies.

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Author Profile

Mrs. Lekshmi Vijayan is PG research scholar at TKMIT, Kollam. Her area of interest includes VLSI design and engineering.
Mrs. Sukanya Sundaresh is assistant professor at TKMIT, Kollam. Her subject area includes VLSI design & Engineering.