delay of the XOR, OR, latch and the AND gate must not exceed the setup time of the FF. Such constraints may exclude 5%-10% of the FFs from being gated due to their presence on timing critical paths. The exclusion percentage increases with the increase of critical paths, a situation occurring by downsizing or turning transistors of non-critical path to high threshold voltage (HVT) for further power savings.

## 3. Auto-Gated Flip-flop

Flip-flops have their content modification solely either at the rising or falling fringe of the modify signal. But, once the rising or falling fringe of the modify signal, the flip-flop's content remains constant even though the input modification. in a very typical D Flip Flop, the clock signal perpetually flows into the D flip-flop no matter whether or not the input changes or not. A part of the clock energy is consumed by the interior clock buffer to manage the transmission gates unnecessarily.

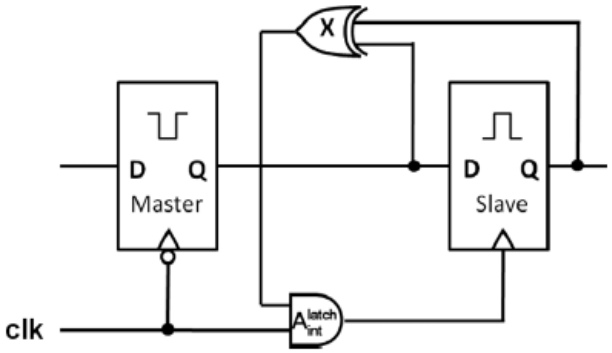


**Figure 2:** Auto-gated Flipflop

Hence, if the input of the flip-flop is the image of its output, the shift of the clock will be suppressed to conserve power. The auto gated flip-flop design has been illustrated in Figure 2. This block consists of master and the slave combination of flip-flops and the latch. The FF's falling edge of the clock pulse could be gives the time prior of the input signal. The XOR gates are to be highlighting the state of the slave latch when it could be enabled. The sectional view of this latch and the flip-flop can be having the timing constraints when compared to the data driven clock gating. The level of the clock signal enables the pulses from the triggering edges of the input. The gating can be detected to be critical in the master slave flip-flop enabling.

### 3.1 Drawback of Autogated Flipflops

There are two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

## 4. Look Ahead Clock Gating

Look Ahead Clock Gating computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. Similarly to data-driven gating, it is capable of stop-ping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gate. Furthermore, unlike data driven gating whose optimization requires the knowledge of FF‟s data toggling vectors, LACG is independent of those. AGFF can also be used for general logic, but with two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

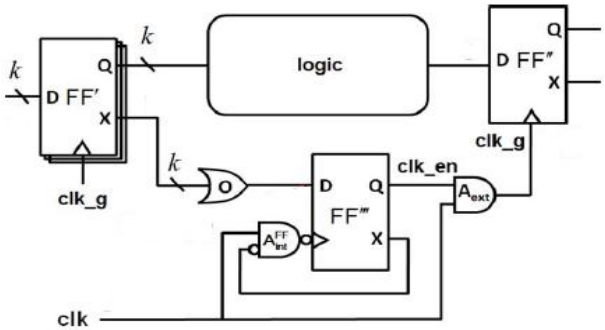


**Figure 3:** Look Ahead Clock Gating Flipflop

LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. LACG is based on using the XOR output in Figure 3 to generate clock enabling signals of other FFs in the system, whose data depend on that FF.

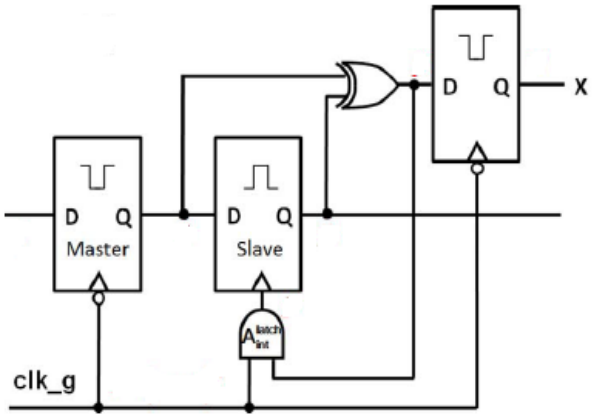


**Figure 4:** Enhanced AGFF with XOR output used for LACG

### 4.1 Advantage of LACG

Look ahead clock gating has been shown to be very useful in reducing the clock switching power. Similar to data driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gate.

## 5. Results

Tanner EDA helps to transform your ideas into design. It has created a software platform that is cost efficient. It is powerful enough to handle complex design. Tanner EDA's continued innovation makes its tools effective solution that grows with a

company as its performance needs change. Tanner EDA consist of various tools namely S-edit, T-spice, W-edit, L-edit and LVS. In S-Edit, schematic design of circuit enables you to check your design for common errors such as undriven nets, unconnected pins and nets driven by multiple outputs so you can catch errors early before running simulations.

T-Spice lets you precisely characterize circuit behavior using virtual data measurements. For greater efficiency and productivity, TSpice controls over your simulation process with an easy-to-use graphical interface. The W-Edit waveform analysis tool is a comprehensive viewer for comparing, displaying and analyzing simulation results. W-Edit is dynamically linked to T-Spice and S-Edit with a run-time update feature that displays simulation results as they are being generated and allows waveform cross-probing directly in the schematic editor for faster design cycles. Layout is essentially a drawing process. L-Edit gives you the flexibility and control you need to master the editing process. LVS (Layout Versus Schematic) compares net list generated by schematic and net list generated by layout. The generated parameters are compared and if found similar then it is an indication that the designed layout is ready for fabrication.

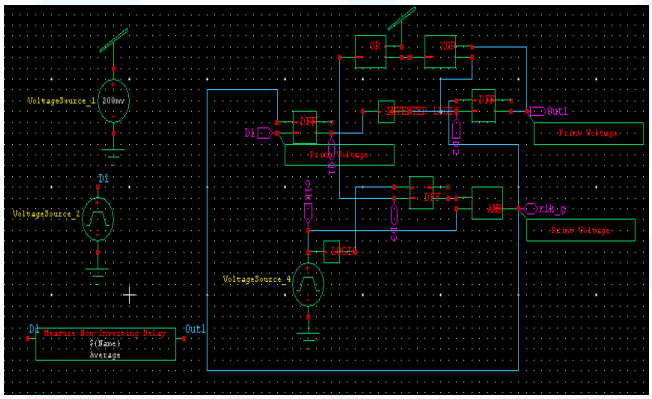

**Figure 5:** Output of Data driven Clock Gating

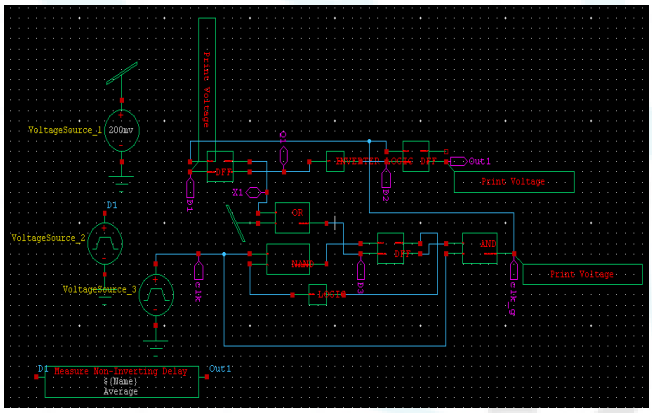

**Figure 6:** Output of Look Ahead Clock gating

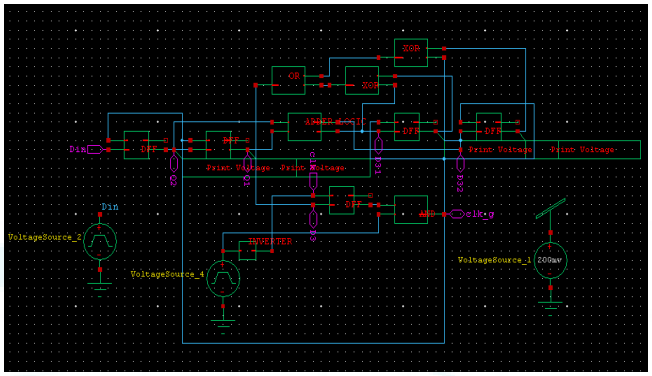

**Figure 7:** Shift register design by using LACG

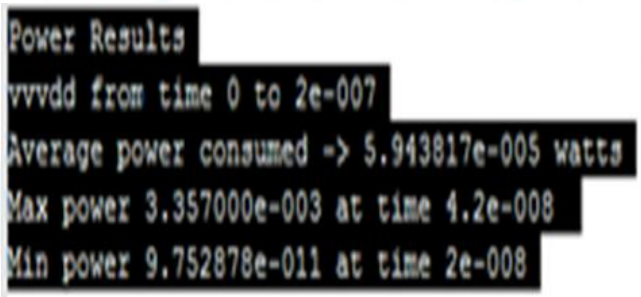


**Figure 8:** Power consumed in the circuit is displayed in the out file

As shown in Table 1, the simulation results clearly indicate that the Shift Register using LACG is faster compared to the other two methods.

**Table 1:** Summary of Simulation Results

| *Circuit* | *Power Consumption* | *Delay* |
|---|---|---|
| Data Driven Clock Gating | 1.931668e-008 W | 6.9005e-009 |
| Look Ahead Clock Gating | 1.322850e-008 W | 8.6123e-009 |
| Shift register design using LACG | 3.018285e-008 W | 6.2025e-009 |

## 6. Conclusion

The Look ahead clock gating has been shown to be very useful in reducing the clock switching power. Similar to data driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gate. Furthermore, unlike data driven gating whose optimization requires the knowledge of FF‟s data toggling vectors, LACG is independent of those and also it is independent of the target application. The power in LACG has been reduced to 50% than the Auto-Gated FF which consumes 50% less power than the data driven method. Clock gating method uses to reduce the Dynamic Power consumption in future we can integrates the static power consumption reduction techniques in-order to reduce the both the losses of CMOS.

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