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A Novel Approach for Auto Clock Gating of Flip-Flops

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Abstract: ***Clock gating is a one of the power saving technique. It is a popular technique used in many synchronous circuits for reducing dynamic power dissipation and extraordinarily helpful for decreasing the ability power wasted by digital circuits. This paper proposes a new technique of look ahead clock gating. It avoids and replaces the drawbacks of the previously existing ways. the present systems for clock gating are synthesis base clock gating, information driven clock gating and clock gating on auto gated flip flops however of these techniques had some disadvantages. This project deals with the replaces the drawbacks within the existing system Look-Ahead Clock Gating (LACG), combines all the three. LACG computes the clock enabling signals of every FF one cycle before time, supported the current cycle information of these FFs on that it depends. It avoids the tight temporal arrangement constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation. The Simulation will be done in Tanner EDA 13.0v T-Spice at 0.18um.***

Keywords: Clock, Gating, dynamic power, Look-Ahead Clock Gating, synchronous circuits

1. Introduction

CMOS Technology is one of the mainstreams of VLSI Design. In 0.18µ and above technology Dynamic power is one of the main factors of total power consumption. But when technology feature size shrinks static (Leakage) power dominates the dynamic power. So however, the designers proposed several methods to reduce the leakage. In Base Technique of Power Gating there is no method for leakage reduction but it saves the state as well as minimum area and delay. Sleep Transistor Technique is most common method for achieving ultra-low leakage but it destroy the state and as well as increasing delay and area.

Forced Stack technique is another method and it can save the state. But in this technique, Dynamic Power consumption is increased and it cannot use high threshold voltage without increasing the Delay. By combing these two prior techniques Sleepy Stack approach is proposed. It reduces the leakage similarly like sleep transistor technique but the main advantage over sleep transistor technique is save the logic state. Moreover, Sleepy Stack approach comes with area and delay overhead and slower method than other technique. However, Sleepy Keeper approach is considerable for propagation delay and static power performances. Variable Body Biasing approach can be used for efficient area and dynamic power dissipation.

In Base Technique of Clock Gating, output correctness problem is present due to glitches and hazards. So for elimination of hazard, we can use the latch based AND Clock Gating. But till now these two common techniques are used. Hence we sought a new method which can have excellent tradeoff between power, area, and delay.

Energy dissipation is a very critical parameter that has to be taken into account during the design of Very Large Scale Integration (VLSI) circuits. With the rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery-operated portable devices a major concern. High power consumption reduces the battery service life. Reducing power dissipation is a design goal even for non-portable devices since excessive power dissipation results in increased packaging and cooling costs as well as potential reliability problems. There are two major forms of design power efficient Complementary Metal Oxide Semiconductor (CMOS) circuits: technology and project choices. The former includes research on new materials, reducing supply, threshold voltages, and doping levels. The latter includes algorithms, data encoding style, the use of pipeline, parallelism, Clock Gating or any other low power technique. This work carries a study on the impact of both topology and technology choices on power consumption of logic gates used in standard cell libraries.

Portable electronic devices tend to be much more complex than a single VLSI chip. They contain many components, ranging from digital, analog to electro-mechanical and electro-chemical. Dynamic power management which refers to a selective shut-off or slow-down of system components that are idle or underutilized has proven to be a particularly effective technique for reducing power dissipation in such systems. Incorporating a dynamic power management scheme in the design of an already-complex system is a difficult process that may require many design iterations, careful debugging and validation.

Integrated Circuit (IC) power dissipation consists of different components depending on the circuit operating mode. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the active component and the standby leakage component. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions or by Power Gating.

One of the most important dynamic power consumers in computing and consumer electronics product is that the

system's clock signal, generally liable for half-hour to 70th of the overall dynamic (switching) power consumption. Many techniques to scale back the dynamic power are developed; of that clock gating is predominant. Ordinarily, once a logic unit is clocked, its underlying serial parts receive the clock signal regard-less of whether or not or not their information can toggle within the next cycle. With clock gating, the clock signals area unit ANDed with expressly predefined signals. Clock gating is used the least bit levels: system design, block style, logic style and gates. Many ways to require advantage of this system area unit represented, with all of them counting on varied heuristics in a shot to extend clock gating opportunities. Gated clock may be a common methodology for reducing power dissipation in synchronous digital system. Victimization this methodology the clock isn't given to the flip flop once the circuit is idle. We have a tendency to decision the on top of ways information driven primarily based. Synthesis-based clock gating is that the most generally used methodology by EDA tools. The use of the clock pulses, measured by data-to-clock toggling quantitative relation, left when the employment of synthesis-based gating should still be terribly low. Fig. one depicts the common data-to-clock toggling quantitative relation, obtained by in depth power simulations of sixty one blocks comprising 200k FFs, taken from a thirty two nm high-end 64-bit chip. Those area unit largely management blocks of the data path, register file and memory management units of the processor. The technology parameters used throughout the papers area unit of twenty-two nm low-leakage method technology.

The dynamic power of a circuit in which all the transistors switch exactly once per clock cycle will be (1/2) CV^2F, if C is the switched capacitance, V is the supply voltage, and F is the clock frequency. However, most of the transistors in a circuit rarely switch from input changes. Hence, a constant called the activity factor ($0 \leq A \leq 1$) is used to model the average switching activity in the circuit. Using A, the dynamic power of a circuit composed of CMOS transistors can be estimated as:

$$P = ACV^2F \quad (1)$$

The importance of this equation lies in pointing us towards the fundamental mechanisms of reducing switching power. The second fundamental scheme is to reduce the load capacitance, C_L. This can be done by using small transistors with low capacitances in non-critical parts of the circuit. Reducing the frequency of operation F will cause a linear reduction in dynamic power, but reducing the supply voltage V_{DD} will cause a quadratic reduction.

Also, dynamic power is proportional to the square of the operating voltage. Therefore, reducing the voltage significantly improves the power consumption. Furthermore, since frequency is directly proportional to supply voltage, the frequency of the circuit can also be lowered, and thereby a cubic power reduction is possible. However, the delay of a circuit also depends on the supply voltage as follows.

$$\tau = kC_L V_{dd}/(V_{dd} - V_t^2) \quad (2)$$

Where τ is the circuit delay, k is the gain factor, C_L is the load capacitance, V_{dd} is the supply voltage, and V_t is the threshold voltage. Thus, by reducing the voltage, although we can achieve cubic power reduction, the execution time increases. The main challenge in achieving power reduction through voltage and frequency scaling is therefore to obtain power reduction while meeting all the timing constraints.

2. Existing Data Driven Clock Gating

To address the above redundancy, a method called Data-driven clock gating was proposed for flip-flops (FFs).There, the clock signal driving a Flipflop, is gated when the FF's state is not subject to change in the next clock cycle. In an attempt to reduce the overhead of the gating logic, several flipflops are driven by the same clock signal, generated by ORing the enabling signals of the individual flipflops. Data-driven gating affected from a very short time-window. The cumulative delay of the XOR, OR, latch and the AND gate must not increased the setup time of the Flipflop.

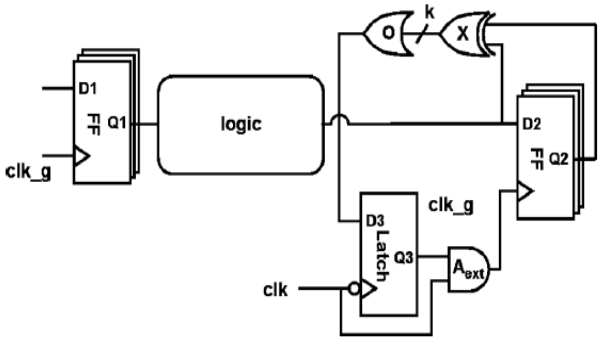

Figure 1: Data Driven Clock Gating

Clock enabling signals are very well understood at the system level and so will effectively be outlined and capture the periods wherever practical blocks and modules don't ought to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In several cases, clock enabling signals are manually accessorial for each FF as a section of a style methodology. Still, once modules at a high logic gate level are clocked, the state transitions of their underlying FFs rely upon the information being processed. It is vital to notice that the complete dynamic power consumed by a system stems from the periods wherever modules clock signals are enabled. Figure 1 one shows the FFs' toggling activity in an arithmetic block comprising designed in 22-nm technology, taken from DSP core for transmission and wireless base band applications The statistics is obtained from intensive simulations of typical modes of operation, consisting of 240-K clock cycles. once the FFs clock signal is enabled is simply 100%, that continues to be accountable for the complete dynamic power consumed by that block. The clock enabling signals are obtained by RTL synthesis and manual insertions. As Figure 1shows, a FF toggled its state solely a pair of.9% of the clock enabled fundamental quantity, on the common, so over 97 of the clock pulses driving FFs are useless.

2.1 Drawbacks of Data Driven Method

Data driven gating suffers from a very short time window where the gating circuitry can properly work. The cumulative

delay of the XOR, OR, latch and the AND gate must not exceed the setup time of the FF. Such constraints may exclude 5%-10% of the FFs from being gated due to their presence on timing critical paths. The exclusion percentage increases with the increase of critical paths, a situation occurring by downsizing or turning transistors of non-critical path to high threshold voltage (HVT) for further power savings.

3. Auto-Gated Flip-flop

Flip-flops have their content modification solely either at the rising or falling fringe of the modify signal. But, once the rising or falling fringe of the modify signal, the flip-flop's content remains constant even though the input modification. in a very typical D Flip Flop, the clock signal perpetually flows into the D flip-flop no matter whether or not the input changes or not. A part of the clock energy is consumed by the interior clock buffer to manage the transmission gates unnecessarily.

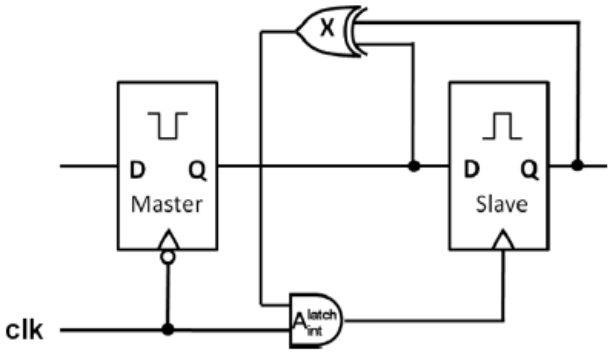

Figure 2: Auto-gated Flipflop

Hence, if the input of the flip-flop is the image of its output, the shift of the clock will be suppressed to conserve power. The auto gated flip-flop design has been illustrated in Figure 2. This block consists of master and the slave combination of flip-flops and the latch. The FF's falling edge of the clock pulse could be gives the time prior of the input signal. The XOR gates are to be highlighting the state of the slave latch when it could be enabled. The sectional view of this latch and the flip-flop can be having the timing constraints when compared to the data driven clock gating. The level of the clock signal enables the pulses from the triggering edges of the input. The gating can be detected to be critical in the master slave flip-flop enabling.

3.1 Drawback of Autogated Flipflops

There are two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

4. Look Ahead Clock Gating

Look Ahead Clock Gating computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. Similarly to data-driven gating, it is capable of stop-ping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gate. Furthermore, unlike data driven gating whose optimization requires the knowledge of FF‟s data toggling vectors, LACG is independent of those. AGFF can also be used for general logic, but with two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

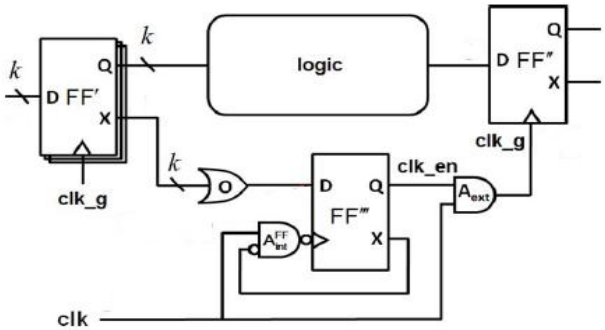

Figure 3: Look Ahead Clock Gating Flipflop

LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. LACG is based on using the XOR output in Figure 3 to generate clock enabling signals of other FFs in the system, whose data depend on that FF.

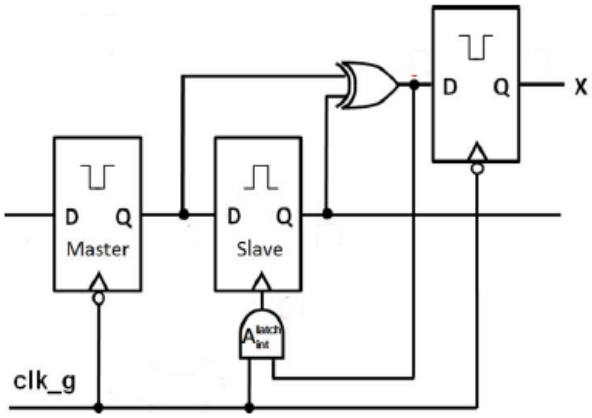

Figure 4: Enhanced AGFF with XOR output used for LACG

4.1 Advantage of LACG

Look ahead clock gating has been shown to be very useful in reducing the clock switching power. Similar to data driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gate.

5. Results

Tanner EDA helps to transform your ideas into design. It has created a software platform that is cost efficient. It is powerful enough to handle complex design. Tanner EDA's continued innovation makes its tools effective solution that grows with a

company as its performance needs change. Tanner EDA consist of various tools namely S-edit, T-spice, W-edit, L-edit and LVS. In S-Edit, schematic design of circuit enables you to check your design for common errors such as undriven nets, unconnected pins and nets driven by multiple outputs so you can catch errors early before running simulations.

T-Spice lets you precisely characterize circuit behavior using virtual data measurements. For greater efficiency and productivity, TSpice controls over your simulation process with an easy-to-use graphical interface. The W-Edit waveform analysis tool is a comprehensive viewer for comparing, displaying and analyzing simulation results. W-Edit is dynamically linked to T-Spice and S-Edit with a run-time update feature that displays simulation results as they are being generated and allows waveform cross-probing directly in the schematic editor for faster design cycles. Layout is essentially a drawing process. L-Edit gives you the flexibility and control you need to master the editing process. LVS (Layout Versus Schematic) compares net list generated by schematic and net list generated by layout. The generated parameters are compared and if found similar then it is an indication that the designed layout is ready for fabrication.

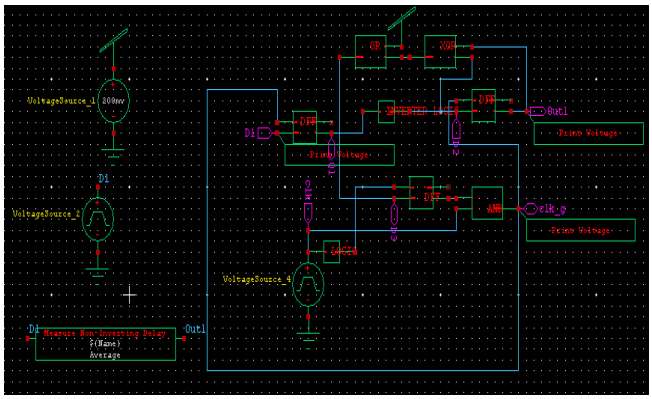

Figure 5: Output of Data driven Clock Gating

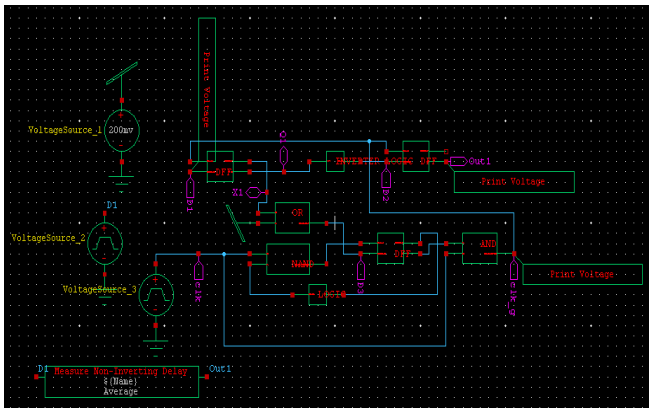

Figure 6: Output of Look Ahead Clock gating

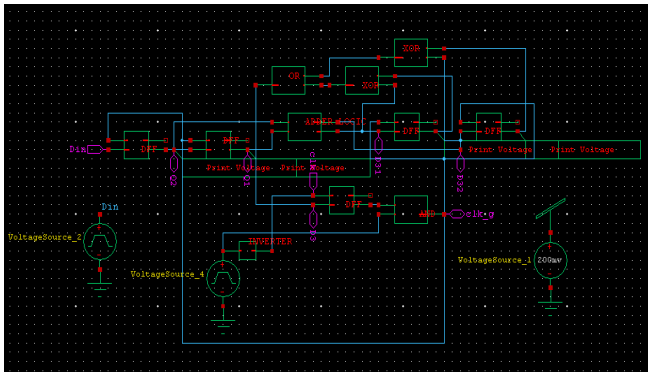

Figure 7: Shift register design by using LACG

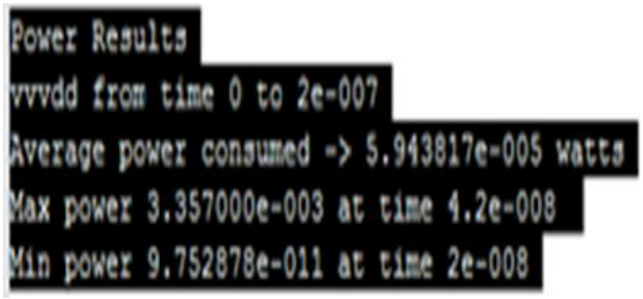

Figure 8: Power consumed in the circuit is displayed in the out file

As shown in Table 1, the simulation results clearly indicate that the Shift Register using LACG is faster compared to the other two methods.

Table 1: Summary of Simulation Results

Circuit	*Power Consumption*	*Delay*
Data Driven Clock Gating	1.931668e-008 W	6.9005e-009
Look Ahead Clock Gating	1.322850e-008 W	8.6123e-009
Shift register design using LACG	3.018285e-008 W	6.2025e-009

6. Conclusion

The Look ahead clock gating has been shown to be very useful in reducing the clock switching power. Similar to data driven gating, it is capable of stopping the majority of redundant clock pulses. It has however a big advantage of avoiding the tight timing constraints of AGFF and data driven, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gate. Furthermore, unlike data driven gating whose optimization requires the knowledge of FF‟s data toggling vectors, LACG is independent of those and also it is independent of the target application. The power in LACG has been reduced to 50% than the Auto-Gated FF which consumes 50% less power than the data driven method. Clock gating method uses to reduce the Dynamic Power consumption in future we can integrates the static power consumption reduction techniques in-order to reduce the both the losses of CMOS.

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