2. e. Addition Unit: The inputs are taken as the output of eight multiplexer units. The output of the eight multiplexers (M7-M0) is added together. The outputs of the adder passes through a two's complement circuit. The produced outputs are varies depending on the sign magnitude and then given to the multiplexer and the outputs are produced.

3. Coefficient Selector (CS) Block

The inputs are taken from the output of the coefficient generator which selects the required data for processing and the selected inputs are multiplied using the AND operation and then based on the multiplexer's selection line, outputs will be produced.

4. Final Data Accumulation Unit (FA)

The inputs for accumulation were taken from the output of the data generator (DG), coefficient generator (CG) and coefficient selector (CS) which are added and then filter output will be produced.

3. Simulation and Results

Finally the 16-bit channel based FIR filter digital architecture was designed. This architecture is used to reduce the noise level in received signal. Then to simulate the final output binary results and to calculate the circuit complexity, power and the speed level.The proposed design has been simulated on ISIM using Xilinx ISE 14.2.The binary data inputs are given and corresponding clock signal is applied either 0 or 1.The waveform are generated to their corresponding inputs. The simulation outputs of the proposed RRC filter architecture is shown in the Fig.3.a and Fig.3.b.

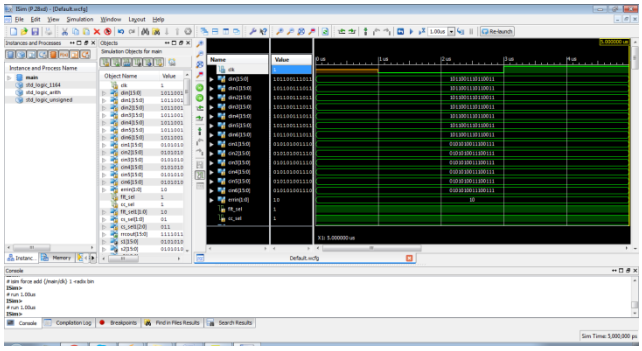

Figure 3.a: Simulation inputs of the proposed reconfigurable RRC filter architecture

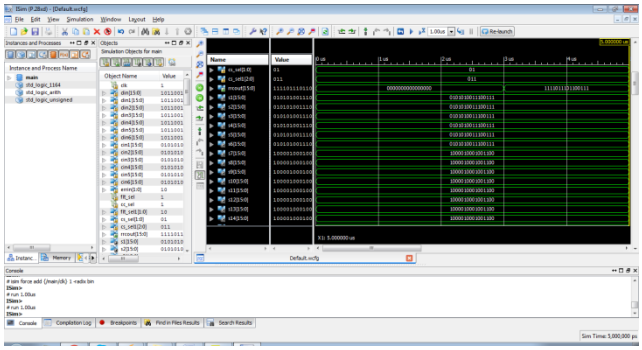

Figure 3.b: Simulation outputs of the proposed reconfigurable RRC filter

After simulation process the proposed design has been implemented using Xilinx ISE 14.2.The Register Transfer Level (RTL) diagram can be implemented for the proposed RRC filter. The simulation and Synthesis Report shows that an efficient Area-Power-delay utilization. The RTL Schematic view of the reconfigurable RRC filter architecture is shown in the Fig.3.c.

Fig.3.c: RTL Schematic view of reconfigurable RRC filter

Total on-chip power as both static and dynamic power can be measured by using Xilinx Power Estimator (XPE)-2013.3.Comparison have been done for the power, delay time, LUT counts and clock frequency of the proposed reconfigurable RRC filter architecture.

Table I: Comparison results of the [9] and proposed reconfigurable RRC filter

References	*LUT counts*	*Delay Time(ns)*	*Maximum .Frequency(MHz)*	*Power (mW)*
[9]	3142	11.9	83.4	231.21
Proposed	2135	9.102	109.8	208

From Table I, it is noticed that the proposed technique helps in reducing LUT counts, Delay time and power along with improvement of maximum frequency compared with [9] existing technique.

4. Conclusion

Finally the FIR with DUC multi-standard channel filter architecture was designed. The circuit complexity level and the delay were reduced. This FIR filter architecture is used to remove the noise in the received channel data bits effectively. This architecture addresses different problems encountered in designing the reconfigurable filter used in multi-standard DUC, which is an important component of Software Defined Radio /cognitive radio. Number of Look Up Table (LUT) counts, path delay and power. This two-step optimization technique to make the desired filter more efficient by reducing area and power along with improvement in operating clock frequency of the design. Comparisons of results of the proposed architecture with other reconfigurable FIR filter architecture implemented on FPGA demonstrate merits of the proposed architecture in terms of speed, power, and area consumption compared to the existing reconfigurable RRC filter architecture. Further the reconfigurable RRC filter architecture is to be enhanced along with an efficient power and area.

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