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A Novel Low Power Pulsed Latch with Increased Reliability

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Abstract: ***The maturation in fabrication technologies of semiconductor integrated circuits results in rapidly shrinking technology node and aggressive scaling of voltage causes an increase in the probability of soft errors in advanced CMOS digital logic circuits. Many attempts to mitigate the soft errors ensue in significant cost penalties in terms of area, power and performance. The proposed method intents a pulsed latch with increased immunity, reliability and reduced power consumption for this purpose, a new transition detector is designed in order to detect single event transition. It shows a remarkable melioration in terms of power, area and performance when compared to conventional transition detector post layout simulation using CMOS 45nm. This detector is further engrafted into the latch to be used as register. The reliability and effectual functioning of proposed pulsed latch is compared with conventional register. The proposed system is designed using MICROWIND 3.1 to get efficacious output.***

Keywords: Reliability, Reduced power consumption ,Pulsed Latch, Transition Detector, Single Event Transition ,Critical Charge, Increased Performance

1. Introduction

Reliability being the major design challenges for the CMOS technology in sub-micron are been impacted greatly by shrinking geometries, lower supply voltages, higher clock frequencies and higher densities [1]

Development of technology causes increase in the density of chip and more over to save power the operating voltage has become lower and lower. All these changes bring a comfortable portable device for us. But as these dimensions and operating voltages of electronic devices are reduced to satisfy the demands of higher density and lower power, circuit becomes more sensitive to externally induced phenomena such as cosmic rays and other high energy particles. One factor of reliability is sensitivity to these external induced particles which makes the circuit more susceptible to spurious voltage variation altering the node voltage values. These are extremely bad for flip flops and latches whose output depends on input data. This affects the integrity resulting in transient fault or single event transition, when latched by a sampling element results in soft error. This soft error occurs when ever the minimum charge deposited in the sensitive node of the flip flop to change the stored bit is less compared to the externally induced cosmic or high energy particles, and is also classified as single event upset in space communication [2-4].

A single event transient (SET) is a transient voltage pulse created due to a single event at a node in an integrated circuit. Under certain conditions, this transient pulse can propagate through the integrated circuit and eventually appear at the circuit's output. It may also be captured if it appears at the input of the latch during the setup and hold time of the latch (also known as (window of vulnerability). A SET, thus

captured, becomes a single event upset. A single event upset (SEU) is a change of state caused by ions or electro-magnetic radiation striking a sensitive node in a micro-electronic device, such as in a microprocessor, semiconductor memory, or power transistors. The state change is a result of the free charge created by ionization in or close to an important node of a logic element (e.g. memory "bit"). The error in device output or operation caused as a result of the strike is called an SEU or a soft error. The SEU itself is not considered permanently damaging to the transistors or circuits' functionality unlike the case of single event latch up (SEL), single event gate rupture (SEGR), or single event burnout (SEB). These are all examples of a general class of radiation effects in electronic devices called single event effects.

An SEU can also be generated within a latch when a radiation event causes enough charge to be collected at a sensitive node in the latch. The minimum charge required to flip the state of the latch is termed as critical charge (Qcrit). Qcrit is a property of the particular circuit and depends on factors such as individual transistor currents and nodal capacitances. There are various soft-error mitigation techniques that can be implemented at the device, circuit and architecture levels. For instance, triple-well and silicon-on-insulator technologies are effective mitigation strategies at the device level, Triple Modular Redundancy (TMR) are mitigation techniques at the circuit-level whereas error correcting codes (ECC) and redundant execution are some of the soft-error mitigation schemes at the architecture-level. [6]

2. Previous Work

Many works have been reported to increase immunity of the registers. Some approaches increase the minimum amount of charge stored in sensitive node for changing the state of latch. For example, SIN-HR register, in which the number of sensitive nodes is reduced using two feedback paths and its modified version called "SIN-HR sub"[10] as in Fig.2(a) was designed for subthreshold region. Triple Modular Redundancy (TMR) [8] latch in Fig.2(b) achieves full immunity. However, it consumes more power, occupies more area and also imposes more delay penalty

The proposed structure improves reliability with lower performance compared to conventional registers. Transition detector designed to satisfy fast reaction that is necessary to mask single event effect.

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If D is high the rise detector circuit becomes active causing the output node Sn connected to it to be ground. This output node which is ground causes other output node Sp of the differential output to go high through Inverter A (INVA). If D falls the node Sp is changed to high through the fall detector circuit and the complemented values of node Sp propagates to node Sn through Inverter B (INVB).

The extra transistors inserted to INVA and INVB ensures leakage reduction and the feedback structure ensues in very fast change of Sn and Sp. The Comparison table shows the average power consumption of the proposed and the conventional transition detector, finally the proposed transition detector also has a smaller area. Hence provides a significant improvement in terms of delay, energy and area.

Table 1: Comparison of Transition Detector

	XOR	Proposed
Power consumption (µw)	.621	.104
Delay (ns)	1.20	0
Number of transistors	25	21

4. Reliable Pulsed-Latch

The purported transition detector is engrafted into a conventional latch presenting a new reliable latch. The TD switches the multiplexer designed using pass transistor on detecting a fierce transition. As TD acts promptly, output of the latch never notices soft error. In case an error occurs in the redundant latch, output never observes it as the output is connected to main latch. Besides the change in TD's value unobserved in output as it switches between two latches maintaining the correct values.

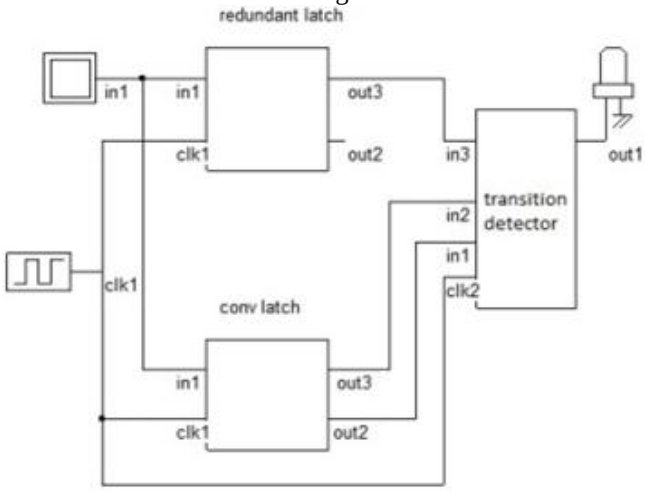

Figure 3 (a): Proposed Latch

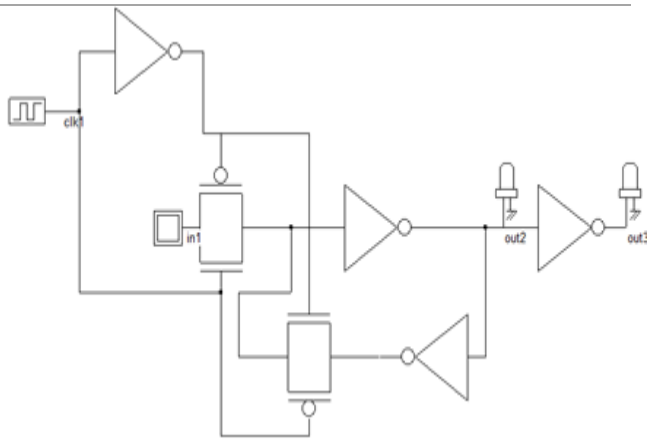

Figure 3 (b): Conventional Latch

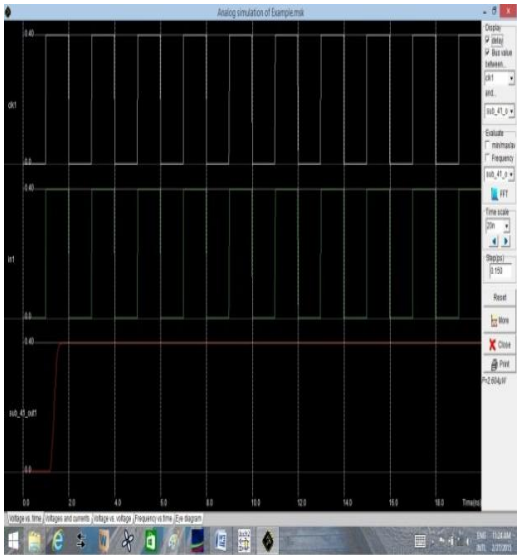

Figure 3 (c): Power Consumption of Proposed Latch

The comparison table shows the average power consumption of the proposed reliable latch, SIN-HR-SUB and TMR. The proposed latch shows least power consumption than the previously existing latches.

Table 2: Comparison of Power Consumption of Proposed Latch

	D-Q Delay(ns)	*Power Consumption (mw)*
SIN-HR-SUB	1.20	0.130
TMR	0.40	0.362
Proposed	0.35	2.604µw

The critical charge for each latch is calculated using (1) so as to model the soft error.

$$I(t)=(Q0/(\tau_t-\tau_f))*(e^{-t/\tau_t}-e^{-t/\tau_f}) \quad (1)$$

Where Q_0 is the collected charge, τ_t is the time constant of collection and τ_f is ion track establishment time constant. The time constant τ_t and τ_f are considered to be 165ns and 50ns respectively. Each node is assigned different values of Q_0 to find the critical charge. This process sequentially is repeated for all nodes of each latch. The following table shows the comparison of robustness of the proposed latch. This shows that the proposed latch comes with increased reliability and better performance.

Table 3: Comparison of Robustness of Proposed Latch

	Critical
SIN-	1.3 (all
TMR	0
Propos	0

5. Conclusion

The proposed design shows increased reliability and better performance on comparing with the previous work in 45nm CMOS technology. The proposed transition detector enhances area occupation, performance and power significantly and the pulsed latch shows inherent immunity to single event transition and least power consumption compared to previous latches.

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