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Design and Simulation of 7-Level Inverter Topology with Fundamental Switching Control

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Abstract: ***Multilevel converters are very interesting alternative for medium and high power applications. Multilevel inverter performs is highly superior when compare to two level inverters because of to reduce harmonic distortion, lower electromagnetic interference and high dc link voltages. Somewhat disadvantages are increases number of components and complex pulse width modulation control method and voltage balancing problem. In this paper a new simplified multilevel inverter topology for generation of seven level of output voltage with less number of switches and good voltage balancing presented and multilevel PWM control scheme used to have a minimum power losses and in this scheme three reference signal and one carrier signal used for generation of gate pulses. Simulation results are presented showing the validity of the analysis.***

Keywords: multilevel inverter, power electronics, PV module

1. Introduction

Multilevel power conversion was first introduced more than twenty years ago. The multilevel inverter has drawn tremendous interest in the power in the power industry [1]. They present a new set of features that are well suited for use in reactive power compensation. By using multilevel inverter to produce quality output voltage or a current waveform with minimum amount of ripple content [2]. It can be possible by using more number of active semiconductor switches to perform conversion in small voltages steps. There are several advantages in process when compare to the conventional power conversion approach [3]. One area where multilevel converters are mostly suitable is that of renewable photovoltaic energy that efficiency and power quality are of concerns for the researchers. Multilevel inverter mostly popular area where the numbers of switches are reduced [4].

The multilevel inverter can be classified in three types one is diode clamped and flying capacitor inverters, it requires the less number of components to achieve the same number of voltage levels. And there are no extra clamped diodes or voltages balancing capacitors. But the small disadvantage in cascaded multilevel inverter needs separate dc source for real power conversion.

In this paper presents overview of a symmetrical seven level inverter topology with reduced number of switches. Where the input is given from photovoltaic module. The multilevel inverter is divided into two parts one is level generator generates the polarity of the output voltage either positive or negative. The proposed topology is simulated using sim power system toolbox of mat lab and the results are presented.

2. Photovoltaic Module Design

The block diagram of MATLAB-simulink based PV module as shown in Fig1(a). the equation describing the characteristics of PV are embedded with three inputs and one output as shown below. Where V_{pv} is the output voltage, T_c is the cell operating temperature, G is the irradiation, I_{pv} is the output current of PV module. A current controlled source is used for simulating the pv module output current. A bypass diode is connected in parallel with current controlled source. All components are embedded into subsystem block as shown in Fig1(b). In this subsystem port out + is the positive terminal and – is the negative terminal of PV module. Port S is the irradiation is cell temperature.

A PV module GS-S-390-TS produced by solarex with 36 sells connected in series.

Standard Test Condition (STC):

Irradiation = 1000w/m^2, air mass = 1.5, cell generating temperature = 25^0 c and wind speed = 1m/s.

Nominal Operating Conditions (NOC):

Irradiation = 800w/m^2 air mass = 1.5, cell operating temperature = NOCT and wind speed = 1m/s. NOCT usually lies between 42^{0}c and 50^{0}c.

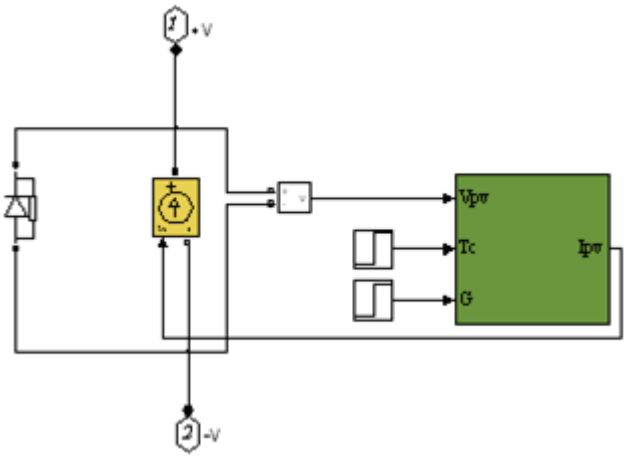

Figure 1 (a)

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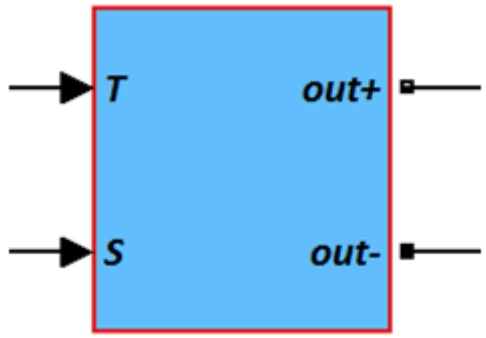

Figure (b)

Figure 1(a) PV module model in MATLAB-simulation block diagram of the PV module (b) PV module sub system.

Table 1: GS-S-390-TS module electrical specifications at STC

Parameters	*Variable*	*Value*
Maximum power	P_{mpp}	390
Voltage at P_{max}	V_{mpp}	40
Current at P_{max}	I_{mpp}	7.92
Short circuit current	I_{sc}	8.65
Open circuit voltage	V_{sc}	44.1

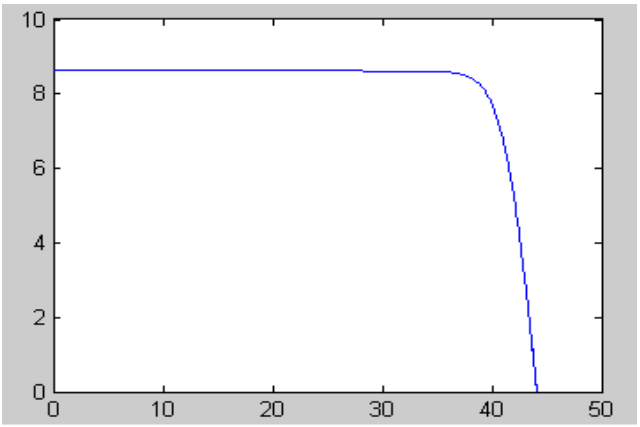

Figure 2 (a): V-I Characteristics of PV module

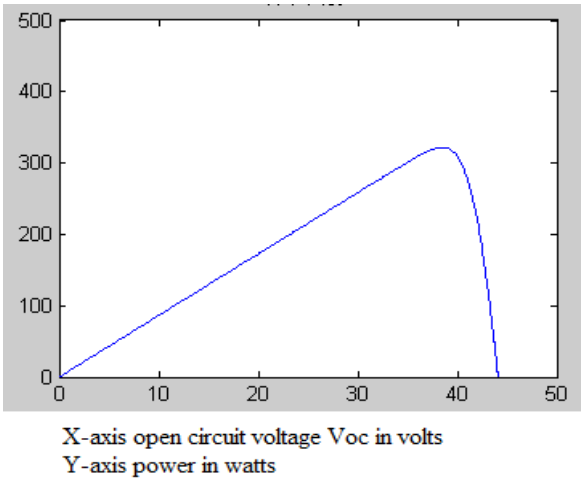

Figure 2 (b): P-V characteristics of PV module

Power Stage: In Fig3 shows that the power circuit of the proposed seven level inverter topology. In conventional multilevel inverters, the power switches are operated to produce a high frequency wave form in both positive and negative polarities. In this level generator switched used high frequency capability for generating required levels. Whereas power switches are used in polarity generator is line frequency capability for generating polarity of output voltage. In the proposed topology fundamental switching scheme is employed in which no high frequency PWM is required.

Block Diagram of Symmetrical Multilevel Inverter:

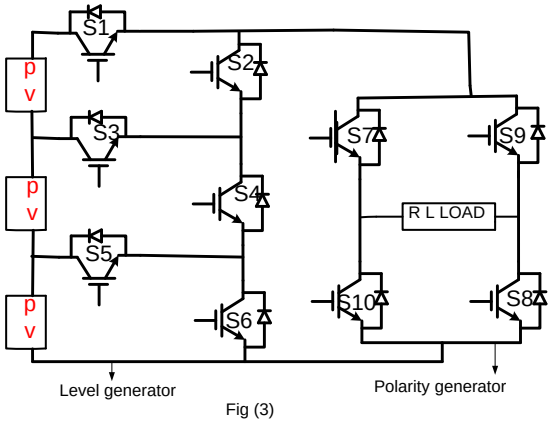

Fig (3)

Power Stage Operation:

Level zero

The switches S_2 S_4 S_6 S_7 S_8 are ON and remaining switches are OFF then short circuit across the output terminals. So zero output voltage is generated.

Level one:

The switches S_2 S_4 S_5 S_7 S_8 are ON and remaining switches are OFF then V_{dc} voltage will be appear across the output terminals.

Level two:

The switches S_2 S_3 S_7 S_8 are ON and remaining switches are OFF then $2V_{dc}$ voltage will be appear across the output terminals.

Level three (peak value):

The switches S_1 S_7 S_8 are ON and remaining switches are OFF then peak (3Vdc) voltage will be appearing across the output terminals.

Table 2: Switching combination required to generate each output voltage level.

Level	*0*	*1*	*2*	*3*
Active Switches	S_2 S_4 S_6 S_7 S_8	S_2 S_4 S_5 S_7 S_8	S_2 S_3 S_7 S_8	S_1 S_7 S_8

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Multilevel PWM Technique:

In multilevel PWM modulation technique used three reference signals those are $V_{ref1,}V_{ref2,}V_{ref3}$ and one carrier signal $V_{cr.}$ Reference signals have the same frequency equal to the line frequency and the same amplitude. They are in phase with each other with the offset value equal to the amplitude of carrier signal. There are three reference signal compare to the carrier signal. . If V_{ref1} take turn when it exceeds the peak of carrier signal V_{cr}. And the V_{ref2} take turn when it exceeds the peak of carrier signal V_{cr}. And V_{ref3} take turn when it exceeds the peak of carrier signal V_{cr} until it reaches to zero. One V_{ref3} reaches zero, V_{ref2} will be compared again until it reaches zero. Onwards V_{ref1} will be compared with carrier V_{cr}.

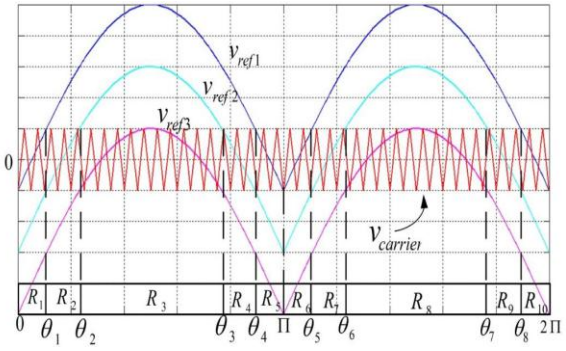


Figure 4

States are determined as follows:

State1: $0 < \omega t < \theta 1$ and $\theta 4 < \omega t < \pi$
State2: $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$
State3: $\theta 2 < \omega t < \theta 3$

Phase angle displacement cab be determined from above fig4.we can observe that at θ1 reference signal and carrier signal are equal. Carrier signal magnitude V_{cr} and reference signal magnitude $V_m \sin \theta 1$. Mathematically can be explained as in below

$V_{cr} = V_m \sin \theta 1$ therefore $\theta 1 = \sin^{-1}(Vcr|Vm)$ and same as θ5.

$$\theta 2 = \theta 6 = \sin^{-1}(Vcr|2Vm)$$
$$\theta 3 = \pi - \theta 2$$
$$\theta 4 = \pi - \theta 1$$
$$\theta 7 = 2\pi - \theta 6$$
$$\theta 8 = 2\pi - \theta 5$$

Modulation index can be determined by using in this inverter. Modulation index can be defined as the ratio of amplitude of reference signal to amplitude of carrier signal

$M_a=(Vm|3Vcr)$
V_m = amplitude of reference signal
V_{cr} = amplitude of carrier signal

In this proposed topology modulation index can be determined as 0.9.

Switching functions:

$S_1 = C_3 * R_3$
$S_2 = \bar{S}_1$
$S_3 = C_2*[R_2+R_4]+\bar{C}_3*R_3$
$S_4 = \bar{C}_2*[R_1+R_2+R_4+R_5]$
$S_5 = C_1*[R_1+R_5]+\bar{C}_2*[R_2+R_4]$
$S_6 = \bar{C}_1*[R_1+R5]$

S_7 and S_8 are ON during positive polarity output. S_9 and S_{10} are ON during negative polarity output. From above switching functions where '+' represent as logical OR gate. '*' represent as logical AND gate. '−'Represent as logical inverse [NOT]. R_x represents the time period of the corresponding region and C_x represents the comparator output. The efficiency of inverter depends up on the number of switching are conducting. Because the numbers of switches are conducting stage are more than the switching losses are more so efficiency are less. In this proposed topology conducting switches lower than the cascaded inverter. So efficiency will be improved.

3. Simulation Result

The multilevel inverter topology simulations are carried out on MATLAB/SIMULINK platform fig5 shows.

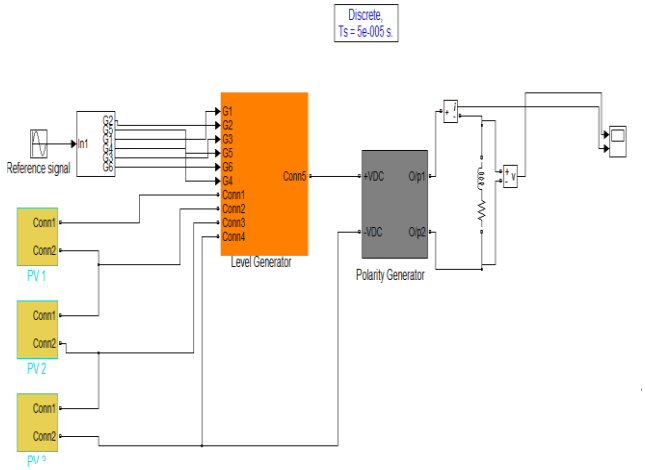
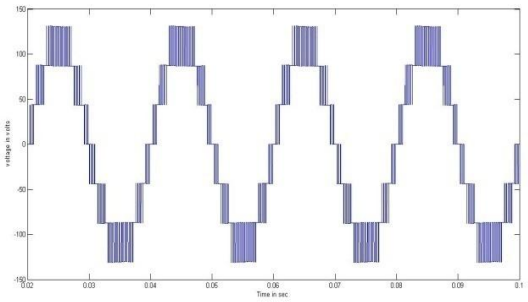


Figure 5: Simulink diagram of symmetrical multilevel inverter topology

The output wave forms of the inverter feeding resistive load 50Ω is shown in figure 6.



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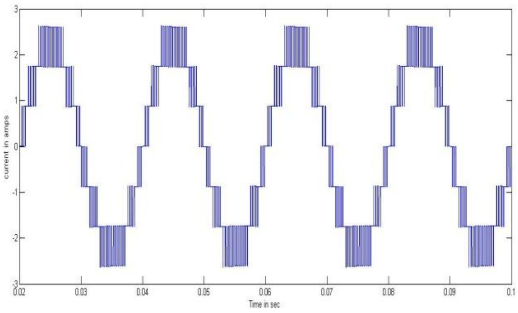

Figure 6: Output voltage level generation [50v/div] and output current [1A/div]

Output wave forms of the inverter feeding resistive [50Ω] and inductive [30mH] load.

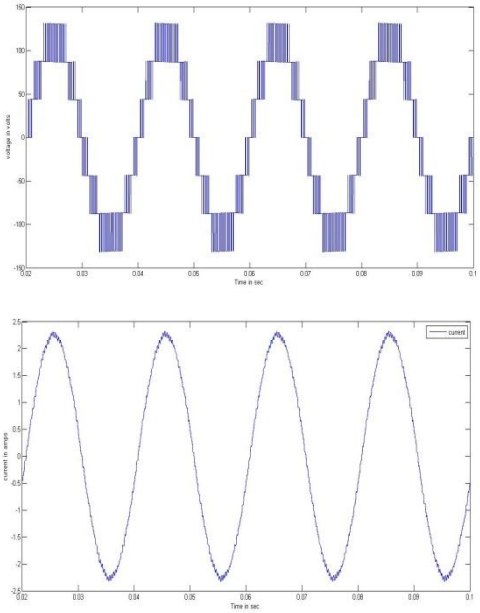

Figure 7: Output voltage level generation [50v/div] and output current [1A/div] as shown in figure 7

The %THD of current is 2.05% without any filtering as shown in figure 8.

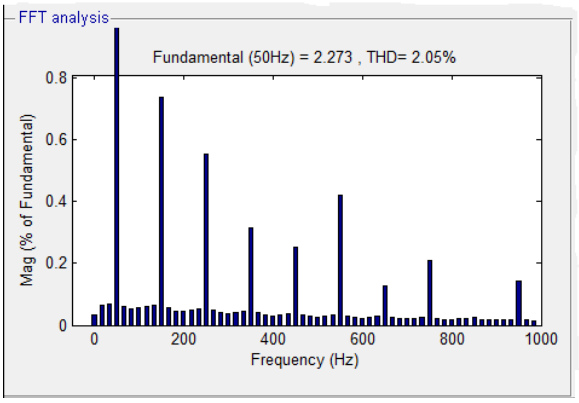

Figure 8: Current waveform THD for seven level of output voltage

Comparator and gate signal generation as shown in figure 9 and figure 10.

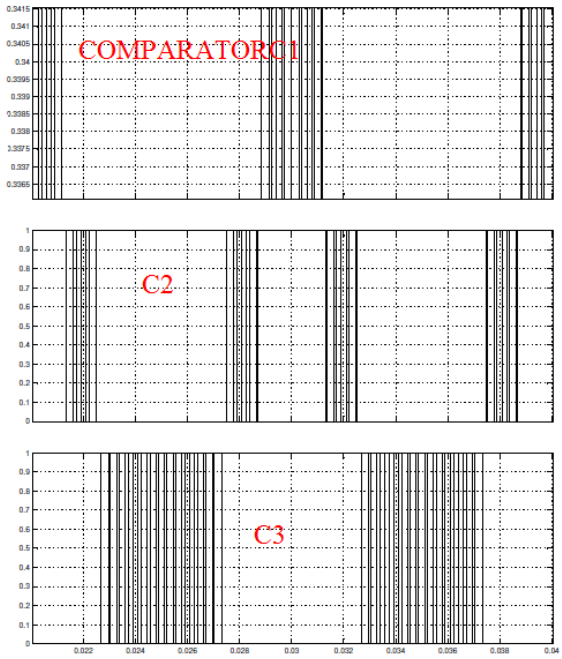

Figure 9: Decision signal produced by the comparator

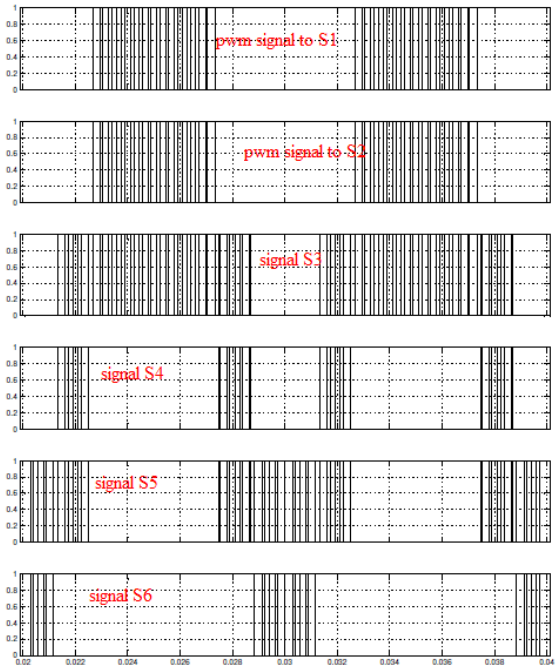

Figure 10: PWM signal generation for seven level generation

Table 3: Comparison of components required for proposed topology with other popular inverters

Multilevel Inverter	*Neutral point clamped*	*cascaded*	*Flying capacitor*	*Proposed topology*
Main switches	12	12	12	10
Main diodes	12	12	12	10
Dc bus capacitor	6	3	6	3
Total number	30	27	30	23

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4. Conclusion

In this paper a new simplified symmetrical multilevel inverter topology performs good and produced output voltage near to sine wave and lower THD value without using filtering. Cost and control system are more reliable. The complexity of PWM technique is low because of it needs to generate the gate pulse for positive only. The number of switches required less for generation seven level and results are clearly and effectively determined.

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