International Journal of Scientific Engineering and Research (IJSER)
www.ijser.in
ISSN (Online): 2347-3878, Impact Factor (2015): 3.791

Implementation of PLC using FPGA

Dhruti Dave[1], Punit Raninga[2]

[1]Parul Institute of Engineering & Technology, Vaghodiya, Gujrat, India

[2] Professor, Parul Institute of Engineering & Technology, Vaghodiya, Gujrat, India

Abstract: ***Programmable Logic Controller (PLC) is most important component in modern manufacturing automation systems. Processor and software have been bottlenecks for improving operational efficiency of PLC. To enhance the PLC performance and flexibility, a new design called "Design And Implementation Of FPGA Based PLC" has been proposed here. The design has been simulated using knowledge of FPGA design tools (such as HDL), to translate, integrate and implement the logic circuit in FPGA. The FPGA based Micro-PLC is based on parallel mechanism, so the proposed design works faster as compared to the conventional PLC. Implementing control logic with FPGA to replace a PLC, response time can be improved while sustaining the flexibility of control. In FPGA side Four- 32 bit 4 stage RISC pipeline Processors based on RUNG- Architecture are designed for dynamically forming and controlling each rung. This design also provides increased flexibility because FPGA offers reconfigurable hardware, increased reliability, better performance and faster scanning time.***

Keywords: PLC, FPGA, HDL

1. Introduction

PLCs have established an important place as control elements for logic control of manufacturing systems.[1] Ladder Diagram is widely used to program PLC, microprocessor decodes and executes the LD program in a sequential and cyclic way, that's why performance of PLC is limited and depends on the length of program and speed of processor. In order to overcome these drawback a new PLC design, a FPGA based PLC is proposed. It can achieve reconfigurable hardware structure and parallel execution advantage. A number of researchers have focused on this field. Miyazawa[2] and Ikeshita et al.[3] developed a very rough manner in 1999 to convert the LD into a program description of a very high speed integrated circuit VHDL. Chen and Patyra[4] designed a VHDL model of the whole system directly from the original system requirements to build a controller. The FPGA based Micro-PLC is based on parallel mechanism, so the proposed design works faster as compared to the conventional PLC. Implementing control logic with FPGA to replace a PLC, response time can be improved while sustaining the flexibility of control. In FPGA side Four- 32 bit 4 stage RISC pipeline Processors based on RUNG- Architecture are designed for dynamically forming and controlling each rung. This design also provides increased flexibility because FPGA offers reconfigurable hardware, increased reliability, better performance and faster scanning time.

2. FPGA Based PLC Design

The main Concept in the development of an integrated environment for efficient conversion of IEC61131-3(ladder diagram and functional block diagram) to IEEE1076.6 (VHSIC Hardware description language) is to develop the software which can convert the conventional input of PLC into the HDL[7][8]. Conventional PLCs are inherently sequential due to implementation of ASIP or micro controller at its core. By applying different range of the Frequencies to Conventional PLCs, the output we get at the higher frequency is null, it stops working. Thus implementation of PLC on FPGA is one of the prospective solutions for this requirement [9]. This further requires better designs and environments with built in reliable verification and validation methods. Once this is achieved than an Integrated Development Environment of any of the FPGA manufacturer can provide a platform by which developers can access all the necessary development tools and components required for FPGA based PLC development[8][10]. The structure of FPGA is reconfigurable so the required circuit can be built as long as a LD program is converted into RTL architecture and downloaded to the FPGA chip. This implementation will perform the same functions as the original PLC with LD, but not in traditional manner. Below fig.1[5] shows the architecture of converter of LD to VHDL.

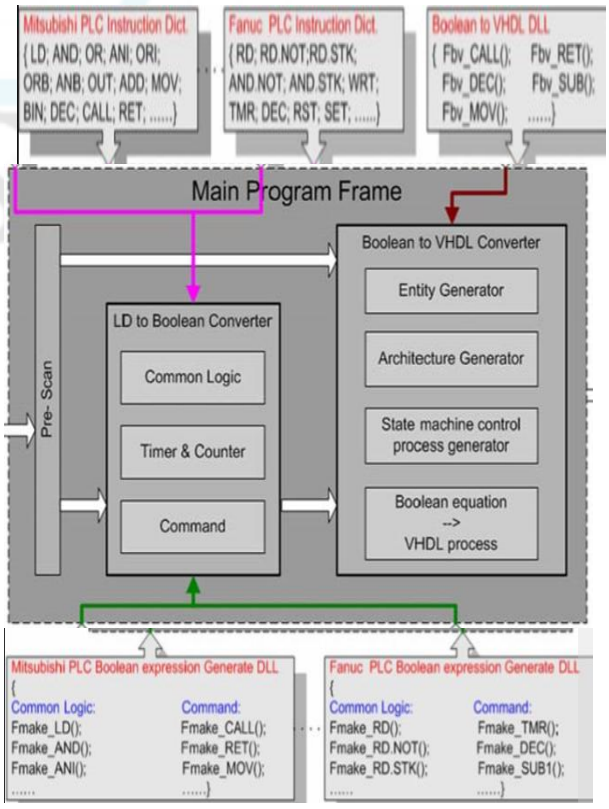

Figure 1[5]: The architecture of converter of LD to VHDL

3. Related Work Approach

One can convert ladder diagram in to c-code usin translation software and that c code is further converted into VHDL code. Main tool is the catapult C high-level synthesis software. As is well-known high-level synthesis is the process of transforming a system level behavioral specification of digital system into register-transfer level structural description implementing that behavior. Catapult C takes as input a functional description of an algorithm in C or System C and produces a VHDL register-transfer level description of a logic circuit, which implements this algorithm. In particular, Catapult C can be used for obtaining optimized designs, because it considers seversl alternative implementations of the algorithm and selects one or more among them according to user-specified criteria.[6]

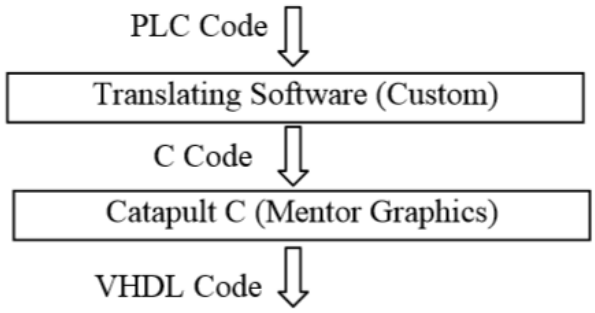

Figure 2[6]: Design Methodology Overview

4. Proposed Work

Here I am using NESYS 2 Spartan 3E family FPGA board and OMERON CP1E PLC for my design. The PLC can be configured by Ladder Diagram using CX programmer which is provided by the manufacturer (OMERON). As per the ladder diagram we have HDL code and FPGA can be configured by that HDL code (bit file) using Xilinx. Now, FPGA generates the different sequences as per the HDL code. The generated output from FPGA is given to the PLC. As per the Ladder Diagram which PLC has it takes the output of FPGA as an input and gave response accordingly. We can check the response of the FPGA and PLC both using Logic Analyzer.

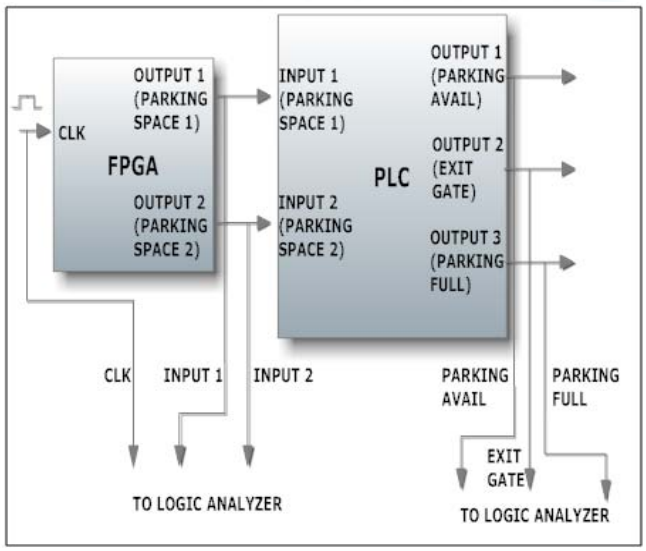

Figure 3: Proposed Architecture

5. Conclusion

At higher complexity (higher clock rate) PLCs can't able to respond. That's why by converting a Ladder Diagram into HDL and then this code can be implemented on FPGA board and further more FPGAs is still find to operate at higher frequencies also. With the help of the HDL code : we have a faster response than conventional PLCs and if we want to check it's functionality with reference to different timings than we don't have to make change in the full code by simply modifying and making proper constraints in the TEST BENCH we are able to check it all. We can't able to do this all by using conventional PLCs.

References

[1] Auslander DM, Pawlowski C, Ridgely J (1998) Reconciling programmable logic controllers with mechatronics control software. Proceedings of the 1998 IEEE international conference on control applications, Trieste, Italy, pp 415–420

[2] Ikeshita M, Takeda Y, Murakoshi H, Funakubo N, Miyazawa I (1999) Application of FPGA to high-speed programmable controller—development of the conversion program from SFC to Verilog. IEEE symposium on emerging technologies and factory automation, Piscataway, NJ, USA, vol 2, pp 1386–1390

[3] Miyazawa I, Nagao T, Fukagawa M, Itoh Y, Mizuya T, Sekiguchi T (1999) Implementation of ladder diagram for programmable controller using FPGA. IEEE symposium on emerging technologies and factory automation, Piscataway, NJ, USA, vol 2, pp 1381–1385

[4] Chen J, Patyra MJ (1994) VHDL modeling of a multivariable fuzzy logic controller hardware system. IEEE international conference on fuzzy systems. Piscataway, NJ, USA, vol 1, pp 129–132

[5] D. Du,Y. Liu:X. Guo:K. Yamazaki Department of Mechanical & Aeronautic Engineering, IMS-Mechatronics Laboratory, University of California, Davis, CA 95616, USA

[6] Christoforos Economakos*, George Economakos† *Halkis Institute of Technology, Department Of Automation, GR 34400, Psachna, Evia, Greece †National. Tech. Univ. of Athens, School of ECE, uLab, Iroon Polytexneiou 9, GR 15780, Athens, Greece,IEEE-2008

[7] Adamski M, Monteiro JL (2000) From interpreted Petri net specification to reprogrammable logic controller design. IEEE international symposium on industrial electronics, Puebla, Mexico, vol 1, pp 13–19

[8] Adamski M (1998) SFC, Petri nets and application specific logic controllers, Proceedings of the IEEE International Conference on Systems, Man and Cybernetics. IEEE, Piscataway, NJ, USA 1:728–733

[9] Uzam M, Jones AH (1998) Discrete event control system design using automation Petri nets and their ladder diagram implementation. Int J Adv Manuf Technol 14(10):716–728

[10] Lee JS, Hsu PL (2005) An improved evaluation of ladder logic diagrams and Petri nets for the sequence controller design in manufacturing systems. Int J Adv Manuf Technol 24(3–4):279– 287