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# Study on Performance of 22nm Single Gate and Multi-Gate MOSFET

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**Abstract:** ***Scaling down of the MOSFET for better circuit density give rise to issues of poor gate control over the dependent current. Many short channel effects contribute towards indeterminist response of the drain current and eventually poor circuit performance. This effects can be overcome if the short channel effects are minimized by gate excitations and by using multiple such gates and there by providing better control over the device parameters. The gate electric field in single gate MOSFET is decreased, and multiple such gates are grown on same substrate so as to have better control over drain current, called as Multi-Gate MOSFET or FinFET. We have recreated the 22nm single gate MOSFET and same channel length multi-gate MOSFET, their performance through various parameter comparisons are evaluated and studied.***

**Keywords:** Circuit density, FinFET, Double Gate MOSFET, Threshold, Electric Field

## 1. Introduction

Scaling of device dimensions has been the primary factor driving improvements in integrated circuit performance and cost, which have led to the rapid growth of the semiconductor industry. Scaling planar CMOS to 10nm and below would be exceptionally difficult but not completely impossible, due to electrostatics, excessive leakages, mobility degradation, and many realistic fabrication issues. Particularly, control of leakage in a nanoscale transistor would be critical to high performance chips such as microprocessors. Non-planar MOSFETs provide potential advantages in packing density, carrier transport, and device scalability. Fin FET is one of the candidates for CMOS device structure in 22 nm technology node and beyond, because of its good cut-off characteristics, better scalability by double gate mode operation, Good gate control over channel, Robustness against short channel effect, Superior scaling, higher current Drive ability and good sub- threshold swing. When we shrinking further the size of the planar MOSFET technology several short channel effects are produced. So instead of planar MOSFET technology DG- MOSFETs technology based on multiple gates device have better controlling over the SCEs. Particularly the Fin FET technology provides superior scalability of the DG-MOSFETs compare to the planar MOSFET. It provides better performance compare to the bulk Si- CMOS technology. Because of its compatibility with the recent CMOS technology Fin FETs are seen to be strong candidate for replacing the bulk or planar Si-CMOS technology from 22nm node onwards. Many different ICs like digital logic, SRAM, DRAM, flash memory etc. have already been demonstrated. Due to their better controlling over sub threshold leakage current and current saturation Fin FETs are advantages for the high gain analog applications and get better result in the RF applications. FinFET on bulk

Si substrate (bulk-FinFET) has many advantages compared to the FinFET on SOI substrate, such as lower wafer cost, Better substrate heat transfer rate and the ease of the combination with conventional planar bulk CMOS devices. There are few reports of successful fabrication of bulk-FinFET with gate length of less than 50 nm, because the control of fin shape and the design of impurity profile in fin area are essential for bulk-Fin FET miniaturization[6].

## 2. MOSFET Scaling and Limits

Scaling of MOSFETs has been followed since the time of its invention. It yields the following advantages:[6]

- Increase in packing density and chip functionality.
- Increase in device current and speed.
- Lower cost (increase cost effectiveness).
- Increase in operating frequency.
- Reduction in power dissipation and gate delays.

But in order to gain these advantages, one has to compromise for different factors which are also called as short channel effects[6]:

- Mobility Degradation,
- Subthreshold Current,
- Variation of Threshold Voltage,
- Drain-Induced Barrier-Lowering (DIBL),
- Drain Punch Through,
- Hot Carrier Effect,
- Surface States and Interface Trapped Charge.

These effects are eminent after scaling due to the high electric field within a very short channel gap. This electric field proves high enough hamper the desired functioning of the device. High electric field within the channel arises the sub-threshold current, which is un-deterministic in nature and keeps device in conducting state even if gate to source voltage is lower than the threshold voltage. Apart from this there are many effect that takes place into a short channel device which is as mentioned above. Just by scaling the applied voltage we cannot insure reliable operation practically. For all practical purposes, it seems impossible to scale the dimensions of classical “bulk” MOSFETs below

20nm.[6] Hence FinFET technology, which replace the device technology itself proves satisfactory for operation.

### 2.1 Multiple Gate (MuGate) MOSFET

With an aim of having better control over the current drive and short channel effects the novel approach in is fabrication itself can provide better results. One such devices are called as Mutligate MOSFET. These are the MOS devices with more than one gate and there by dividing the electric filed in no. of gates grown. Following are the types of multi-gate Devices:

- Single gate MOSFET
- Double gate MOSFET
- Triple gateMOSFET
- Quadruple gateMOSFET

In this study we have realized single gate and double gate MOSFET in 2 Dimension. Their performance based on parameters is compared.

## 3. Simulation of FinFET using Visual TCAD (COGENDA) and its benchmarking

As the dimensions of transistors shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the "short-channel effects" start plaguing MOSFETs. Short-channel effects are the consequences of the leverage of drain to source electric field on the channel than the gate electric field.[6]Voltage-Doping Transformation model (VDT) is a simple tool that can be used to translate the effects of shrinking device parameters such as gate length or drain voltage into electrical parameters[3]. In the particular case of the Short-Channel Effect (SCE) and the Drain-Induced Barrier Lowering (DIBL), the following expressions can be derived from the VDT model[2] :

$$SCE = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} \equiv 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\,V_{bi}$$

$$DIBL = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} \equiv 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\,V_{DS}$$

where $L_{el}$ is the electrical (effective) channel length, $V_{bi}$ is the source or drain built-in potential, $t_{ox}$ is the gate oxide thickness, $x_j$ is the source and drain junction depth and $t_{dep}$is the penetration depth of the gate field in the channel region, which is equal to the depth of the depletion region underneath the gate in a bulk MOSFET. The parameter EI is called the "Electrostatic Integrity" factor. It depends on the device geometry and is a measure of the way the electric field lined from the drain influence the channel region, thereby causing SCE and DIBL effects. Based on the above expressions, the threshold voltage of a MOSFET with a given channel length Lel can be calculated using the following relationship[6][3]:

$$V_{TH} = V_{TH\infty} - SCE - DIBL$$

Where, VTH∞ is the threshold voltage of a long-channel device. The decrease of hreshold voltage with decreased gate length is a well-known short channel effect called the "threshold voltage roll-off". It can be seen that short-channel effects can be minimized by reducing the junction depth and the gate oxide thickness. They can also be minimized by reducing the depletion depth through an increase in doping concentration. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. In that case, most of the electric field lines from the source and drain terminate on the buried ground plane instead of the channel region. This approach, however, has the inconvenience of increased junction capacitance and body effect.

In a double-gate device, both gates are connected together. The electric field lines from source and drain underneath the device terminate on the bottom gate electrode and cannot, therefore, reach the channel region. Only the field lines that propagate through the silicon film itself can encroach on the channel region and degrade short- channel characteristics. This encroachment can be reduced by reducing the silicon film thickness.Electrostatic Integrity(EI) factor of a bulk device can be written as:

$$EI = \left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}$$

### 3.1 Current Drive in Multi-gate MOSFETs

In a multi-gate FET the current drive is equal to the sum of the currents flowing along all the interfaces covered by the gate electrode. It is, therefore, equal to the current in a single-gate device multiplied by the equivalent number of gates provided carriers should have the same mobility at each interfaces. Multi-fin devices are used to drive larger currents. The current drive of a multi-fin MOSFET is equal to the current of an individual fin multiplied by the number of fins [1][4].

### 3.2 Corner Effect

Devices with a triple, quadruple, Ω or ∏ gate structure present a non-planar silicon/gate oxide interface with corners. It has been observed that prematureinversion can form in at the corners of SOI structures because of charge-sharing effects between two adjacent gates. This leads to the presence of two different threshold voltages (one in the corners and at the top or sidewall Si-SiO2 interfaces), as well as a kink in the subthreshold $I_D$-$V_G$ characteristics [1]. The presence of corners can thus degrade the subthreshold characteristics of a device. The easiest way to avoid this problem is to keep a hard mask at the top of FinFET. To go deep into the matter, the radius of curvature of the corners has a significant impact on the device electrical characteristics and can decide whether or not a different threshold voltage will be measured at the corners and at the planar interfaces of the device.[6] One can vary the radius of curvature of the corners and set an optimum value to resolve corner effect.CAD in VLSI plays vital role allowing us to assume any combination of device structure. We has realized 2D model of MOSFET with following dimensions as show in Table 1. 22nm length of the channel is formed by diffusing the drain and source 2nm apart. Planer MOSFET is

assumed and subjected to simulation. MOSFET consisting a $t_{ox}$ layer as the gate insulation with aluminum as gate electrode. Planer MOSFET has this arrangement only on the top of the device. Rather than in Double gate MOSFET, which is realized by producing another gate at the bottom called as $b_{gate}$ and top gate as $t_{gate}$. In MOSFET the gate voltage dependent current $I_D$ is given by schokely's non-linear set of equations. And the threshold voltage in long channel MOSFET is given as:

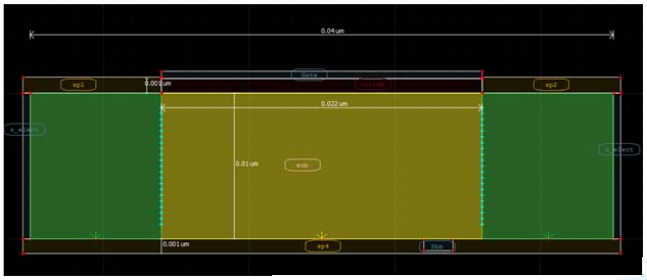

**Figure 1:** Structure of Planar MOSFET of channel length 22nm

N-channel Single Gate and Double Gate MOSFET are assumed. The channel length is tha actual identity of the MOS Technology. Here 2nm are considered for simulations.

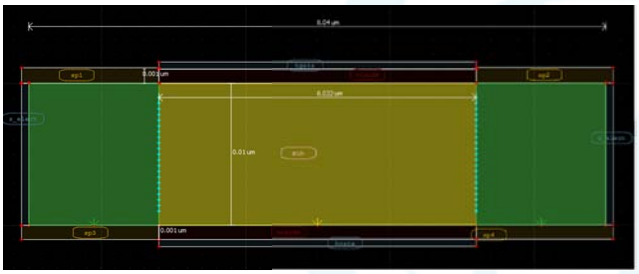

**Figure 2:** Structure of Double Gate MOSFET of channel length 22nm

**Table 1:** Device parameters for simulations

| *Parameter* | *Value* |
|---|---|
| Gate Length | 22nm |
| ChannelWidth | 12nm |
| Fin Height | 40nm |
| Source/Drain Extension | 40nm |
| Source/Drain HDD(total) | 56nm |
| Source/Drain HDD length | 56nm |

## 4. Results

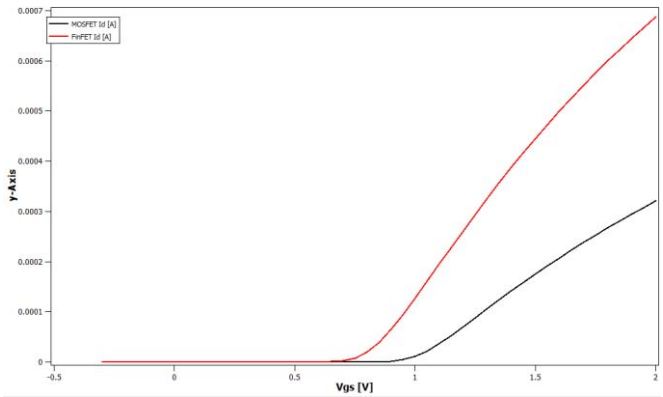


**Figure 3:** Comparison of $I_D$ v/s $V_{GS}$

Devised single Gate MOSFET holds a threshold voltage of 0.95Volt. Whereas the Double gate MOSFET due to current conduction in both top and bottom gate give a threshold voltage of the device as 0.75V. Thus making the device more ideal MOSFET. This is due to the formation of parallel conduction path as compared to the single gate MOS. The slope of drain current is almost double indicating higher trans conductance. Hence this structure provides high current capacity and low threshold voltage features.

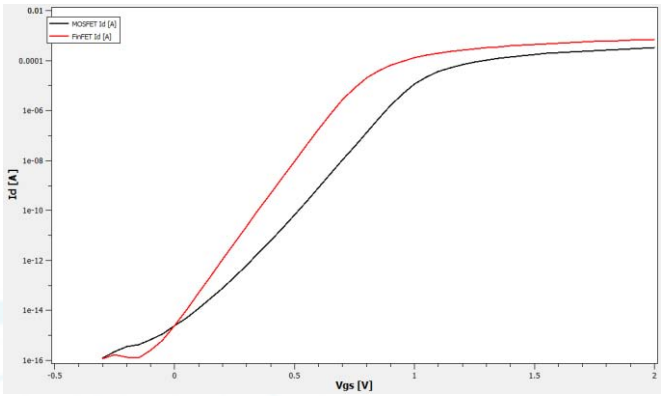


**Figure 4:** Sub threshold Slope (@$V_{DS}$=0.1V)

Sub-threshold region is that operating region when the drive current is measure in log scale and gate voltage lower to that of its threshold voltage is applied. Small amount of current flows even if insufficient gate voltage is applied. This hampers the device functionality and does not make device OFF. Thus continuous power dissipation and lower life. Double Gate proves to have higher sub-threshold slope, which signifies lower sub-threshold current conduction. As compared to planer MOSFET, double gate MOSFET is immune to sub-threshold currents.

**Table 2:** Device performance parameters for simulations with MOSFET and FinFET

| Type | Ion | Ioff | Vth | Ion/Ioff | SS | gm |
|---|---|---|---|---|---|---|
| MOSFET | 0.320524e-3 | 2.46813e-15 | 0.95 | 1.29865e11 | 4.541e-7 | 3.5545e-4 |
| FinFET | 0.687522e-3 | 2.47063e-15 | 0.75 | 2.782780e11 | 3.174e-8 | 6.64e-4 |

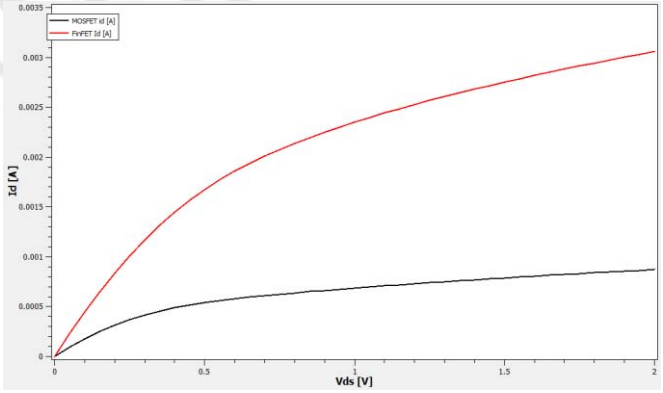


**Figure 5:**Comparison of $I_D$ v/s $V_{DS}$ of MOSFET & Double Gate MOSFET

## 5. Conclusion

Initial Simulation portrayed the improvement in the characteristics making the short channel device easy to fabricate and more ideal.

Decrease in threshold voltage of the device encourages its use for low voltage and low power applications.

Current drive i.e. trans-conductance is nearly doubled.

The leakage current or the sub-threshold characteristics is drastically improved for 22nm Double gate MOSFET.

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