International Journal of Scientific Engineering and Research (IJSER)
ISSN (Online): 2347-3878
Index Copernicus Value (2015): 62.86 | Impact Factor (2015): 3.791

Area Efficient Full Adder Design for Low Power Application

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Abstract: ***In this paper, hybrid logic style is adopted to design the full adder. The main objective of this design is to achieve low power and high speed. Hybrid logic style used is the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG) logic. The circuit was implemented using Microwind tool in 90nm technology.Performance metrics of power and speed are compared with existing adder designs such as conventional CMOS adder, Transmission gate adder (TGA). Average Power consumption of the proposed design is found to be 0.265 µW at 90nm for 1.2V supply. .Delay in the signal propagation is measured as 0.008ns.***

Keywords: CMOS, VLSI, Adder, Transmission Gate Adder, Conventional CMOS Adder

1. Introduction

Increased demand for battery operated portable devices like smart phones, tablets; notebook PC (personal Computer) [8] demand energy efficient designs. Hardware used in these devices has to deliver optimal performance with low power consumption as the amount of battery drain has direct impact on device Performance. Very Large Scale Integration (VLSI) technology is scaled down to accommodate more transistors in given chip area. Large circuit densities enhance the performance at the expense of more energy consumption.

Adder is almostpresent in all computing devices such as Digital Signal Processors, Microprocessors; ALU (Arithmetic Logic Unit) [3].Adder has critical impact on the performance of every digital computing hardware. Fundamental block used to design adder is full adder. Efficient performance of the adder can be obtained by optimizing Full adder. Full adder is the basic building block for other arithmetic circuits such as multipliers and counters. Performance of full adder has direct impact on all arithmetic circuits. Thus energy efficient full adder design is crucial to achieve optimal performance in computing hardware.

2. Design Methodology of Hybrid Logic

Basic cell of Full adder is XNOR/XOR [3] gates. Modular approach is adopted to design Full adder. Hybrid logic is applied to design the SUM module and CARRY generation module. SUM module is constituted of modified XOR gates and carry generation module. SUM module is designed using CMOS logic and Pass transistor logic and Carry module is devised from transmission gates logic. Transistor resizing technique is embedded into the Hybrid logic design for optimality.

3. Design Methodology for Sum Module

Conventional CMOS [9] logic is adopted for designing XNOR gate. XOR gate design requires 4 transistors as represented in Fig.1.The main objective of embedding transistor resizing technique is to minimize the power consumption and to suppress voltage degradation. MP1 and MN1 transistor widths are made small to lower node capacitances thus reducing the power consumption. To realize SUM function two XOR modules are cascaded.

4. Design Methodology for Carry Generation Module

Carry generation module is formulated using transmission gate logic with 4 transistors as shown in Fig.2. Transistor resizing technique [6] is adopted to reduce the delay of carry propagation. Carry is propagated through transistors MP4 and MN4 thus reducing overall carry propagation path. In conjunction to this the widths of transistors MP4, MN4, MP5 and MN5 are broadened to reduce the propagation delay of the carry signal hence enhances the speed.

5. Operation of Full Adder Design Using Hybrid Logic

Full adder design is implemented by integrating the SUM generation module and carry generation module as shown in Fig. 3. Hybrid logic is evident in the design as a combination of conventional CMOS logic (SUM) and Transmission gate

logic (CARRY) with embedded transistor resizing. Boolean expression for sum (1) and carry evaluation (2) is enumerated as follows

$$\text{Sum} = (A \oplus B).\overline{C_{in}} + \left(A \overline{\oplus} B\right).C_{in} \quad (1)$$

$$C_{out} = \left(A \overline{\oplus} B\right).A + (A \oplus B).C_{in} \quad (2)$$

Transistors MP1, MN1, MP2 and MN2 perform XOR [11] Operation with input signals. MP3 and MN3 are employed to implement XNOR operation. Transistors MP4, MN4, MP5 and MN5 are used to implement the SUM expression and transistors MP4, MN4, MN5 and MP5 are deployed to realize carry expression.

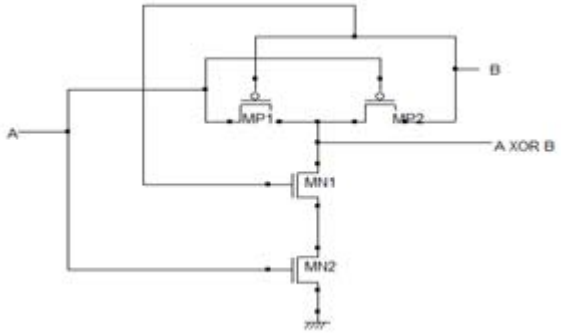

Figure 1: XOR module

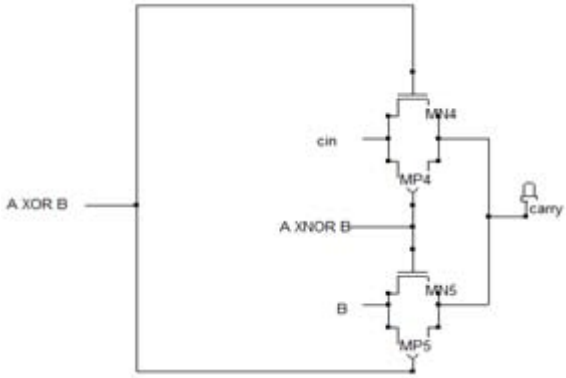

Figure 2: Carry Generation module

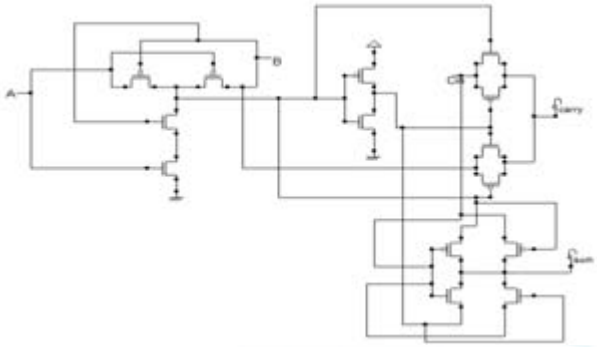

Figure 3: Full adder design with integrated sum and Carry module

6. Circuit Level and Layout Level Implementation of Full Adder Using Hybrid Logic in 90NM

With hybrid logic is realized in circuit level with transistor resizing technique [6] as shown in Fig.5. Layout level of this design is implemented in 90nm for delay evaluation as shown in Fig. 6. Design is carried out in 90nm to analyze the performance in technology scaling scenarios.

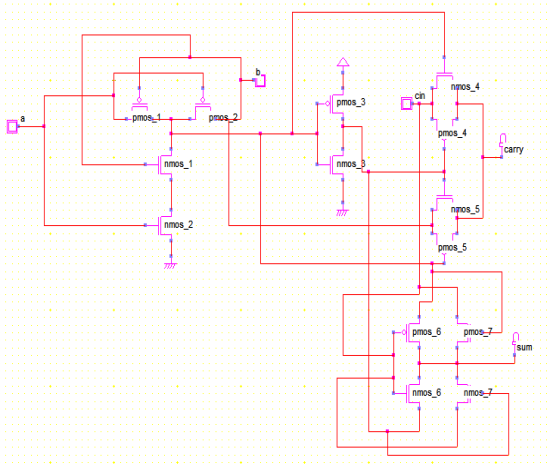

Figure 4: Circuit level Implementation of hybrid logic full adder.

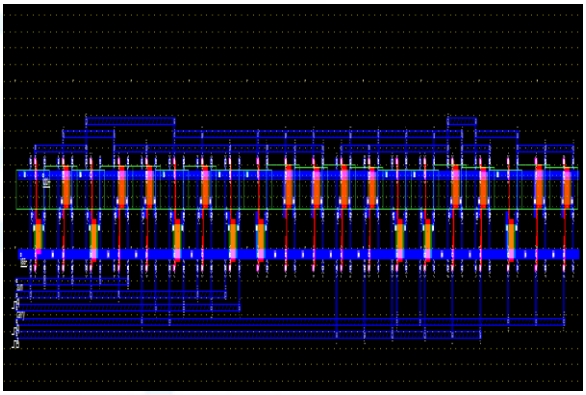

Figure 5: Layout level implementation (90nm)

Circuit level realization of complementary CMOS [3] full adder with 28 transistors is shown in Fig. 8. TGA [8] adder with 20 transistors is shown in Fig.9

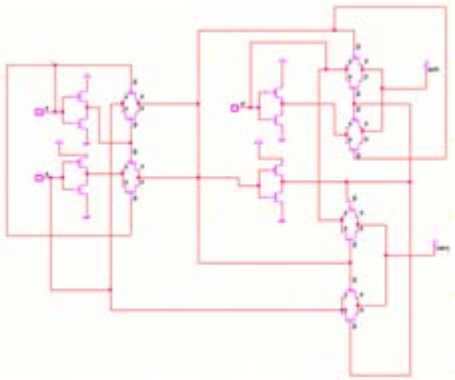

Figure 6: Circuit of Transmission gate Full adder

7. Results

Simulations for various full adder circuit designs are carried out using Microwind tool 3.5 at 90 nm technology output waveforms of Complementary CMOS in Fig.7 andTGA output waveforms in Fig. 8 and Fig. 9 present acceptable voltage swing in the signals.

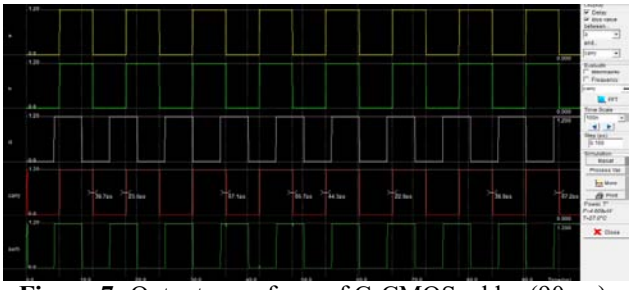

Figure 7: Output waveform of C-CMOS adder (90nm)

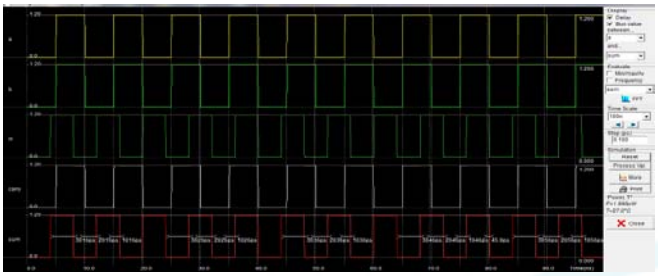

Figure 8: Output waveform of TGA adder (90nm)

Poor voltage swing evident from the simulated waveforms in fig8 . Voltage degradation is enhanced in 90nm. Thus scaling further can affect signal voltage levels to great extent.

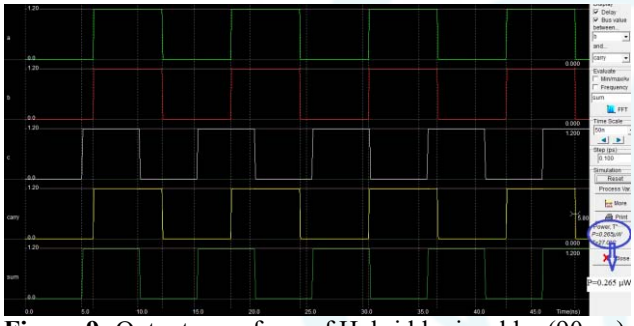

Figure 9: Output waveform of Hybrid logic adder (90nm)

Table 1: Transistor Count, Propogation Delay and Power, Required For Various Logic Designs

Logic Design	Number of Transistors used	90 nm Measured in µW	90 nm Measured in fJ
C-CMOS	28	4.609	0.442
TGA	20	1.998	0.385
HYBRID LOGIC	14	0.265	0.0021

8. Conclusion

Hybrid logic design delivers most efficient performance among other full adder designs is evident from power comparison table. Hybrid logic consumes 6x times less power than complementary CMOS in 90nm TGA consumes 4.8x times more power than hybrid logic in 90nm technology. TFA consumes 4x times more power in 90nm than hybrid logic. Thus hybrid logic consumes less power than all logic designs.

Delay evaluation signifies the speed of the signal propagation in the circuit. C-CMOS logic is 88% slower in than hybrid logic.TGA is 90% slower in 90nm and 68% slower in logic than hybrid logic. Thus hybrid logic delivers high speed performance in technology scaling scenarios.

Transistor count required for the proposed hybrid logic design is less than the other adder designs. Thus area requirement of this design is minimal. Nodes present in the design are less ensuring minimal static and dynamic power dissipation.

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