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IDDT-Based Fault Detection and Localization in 10-T Sub-Threshold SRAM Memory Array

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Abstract: ***In some of the portable, power crucial and not-timing crucial applications more than 90% of the chip area will be occupied by memories and are powered by batteries. As in few applications batteries cannot be recharged it is very essential to reduce the power consumed by memory in order to increase the battery life time. Such application demand low power memories. In recent years a lot of work has been done on designing sub-threshold memories those can successfully operate at low voltages. However, test methods to unveil physical defects in those new memory architectures have not been fully developed. Existing voltage based test methods fail to cover most of the weak opens and also there is no single test method which can unveil all defects in the memory cell. Moreover, the localization of faulty cell in a memory array is not possible. In this work, a dynamic current based delay testing technique which monitors the time at which the abnormal current appears due to fault is used to locate faults. Through simulations it is also found that the minimum detectable resistance is lesser in the proposed technique and thus defect detection in process technology.***

Keywords: Stability Fault, Transient Current (IDDT), Stability fault, Sub-threshold SRAM, Reliability

1. Introduction

In recent years the demand for energy optimized system has been grown significantly. One of the most straightforward way to reduce power consumption is through reducing power supply voltage. From previous studies it is known that CMOS circuits can be successfully operated in subthreshold region in which supply voltage lies within threshold voltage of a transistor. In this region sub-threshold leakage current is used for all computations. In this region power exponentially reduces at the expense of speed. Hence, using sub-threshold region of operation a significant power saving can be achieved for medium frequency operations.

Operation of SRAMs at a sub-threshold voltage is more challenging than operating digital circuits. At lower V_{dd}, the typical 6T SRAM design faces the following major problems: i) decrease in static noise margin (SNM) ii) decrease of the write margin [3], [4]. Therefore, 6T SRAM bit-cell operating at subthreshold region is more vulnerable to noise and at the same time poor write ability. Also, in order to increase the write margin, the size of the pass transistors in a 6T SRAM bit-cell needs to be increased, which may further worsen the static noise margin. Another problem is that the 6T SRAM bit-cell, a proper combination of the six transistors' sizes are extremely hard to obtain under subthreshold operations. Previous results [5] have shown that the minimum supply voltage for the successful operation of a 6T SRAM cell is 0.7 V in CMOS 65 nm technology.

In order to overcome the problem associated with conventional SRAM cell to operate at subthreshold region, several new SRAM bit-cell designs [6], [7], [8], [9], [10], [11], [12], [13] were proposed. In literature, a significant amount of research effort has been put in developing an effective and economic subthreshold SRAM design. However, the testing methodologies for those new subthreshold memory designs have not been fully developed. In this work, one of the efficient 10T-Sub-threshold SRAM cell [6] is considered as Circuit Under Test(CUT).

Testing memory circuits is quite different from testing logic circuits as memories are more of mixed signal circuits whose faulty behaviours are analogue in nature. A very actual problem is the presence of open defects and especially hard-to-detect weak open defects [2]. Particularly, in Nano-meter scaled technologies where copper metallization is used open defects cause serious problem [3]. As the circuit complexity increases testing and localizing defects faces many challenges. In case of most popular 6T SRAM cell two types of open defects are undetectable with normal functional testing. The first type includes opens which results in data retention faults and second type includes defects which do not cause malfunctioning of the cell, instead, they may cause delay issues. Hence, there is a need to develop efficient test methods to unveil such defects. Some resistive-open defects do not cause failure of the circuit under test (CUT) but introduce a significant delay in the output. An obvious advantage of the delay test is that the defects which left undetected by voltage based testing can be detected. In [4] authors have implemented their idea by studying the ability of I_{DDT} and delay tests to detect resistive-open faults.

The detection of defects based on current waveform is very attractive because of its good observability in the circuit. There are many simple fault detection techniques which uses one of the parameter of the current waveform such as width, average value, peak value of the waveform, charge provided by the waveform and the time at which the current waveform reaches its peak value. But, none of the techniques can localize the defects. Alternatively, delay based current waveform analysis can be used for fault detection as well as localization. In this paper, a new test method is implemented which determine the time at which the abnormal shoot up in the current waveform is observed. This information can be used to locate fault in memory array.

The rest of the paper is organized as follows: In section 2 we provide a general background about stability faults, existing testing schemes. In section 3, new testing methodology to detect and localize the resistive open defects using delay based analysis of current waveform is

detailed. Further, paper is concluded along with simulation results.

2. Background of the Work

1. Stability faults

A stability fault in 6T SRAM cell defined in [5], [6], [7], [8] refers to open defect on the source and drain of the cross-coupled pull-up transistors as shown in figure 1, which may not fail SRAM cell operation under a typical operating condition but may fail under some corner conditions such as significant IR drop, noise, or soft error. As a result, a stability fault may reduce the reliability. Therefore, testing stability faults is one of the most challenging tasks in present SRAM testing. Several test methods have been proposed to detect stability faults with as small resistance as possible.

For traditional 6T SRAM cell shown in Figure 1mainly we need to focus on stability faults present on the source and drain of the pull-up pMOS transistors (MT 2 and MT 4 in Figure 1) and faults located on the pull- down nMOS transistors (such as MT3 and MT5 in Figure 1) can be ignored as they can be detected relatively easily by normal read or write operation. The reason for easy detection of such faults is that the bit-lines in general SRAMs are pre-charged to VDD during a read operation. However, in presence of open defects, nMOS transistors cannot successfully pull down a bit-line, then the pre-charged value will be read out, which is opposite to the expected value. Thus, the defect is detectable. On the other hand, if the pMOS transistors cannot successfully pull up the bit-line due to an open defect, then the pre-charged value just happens to be the expected value and hence the open defect cannot be detected. Hence, the past research efforts have focussed only on defects located on the source and drain of pull-up PMOS transistors. Whereas in case of sub-threshold SRAM shown in Figure 2, defects present on pull-down transistor is more significant than conventional 6T-SRAM cell. Because, 10-T cell has separate read and write path and hence, defect on pull-down transistor will not directly affect the RBL during read operation. The various test methods have been implemented to unveil such stability faults in SRAMs. These test techniques include: 1) Read Equivalent Stress (RES), 2)Severe Write and 3) Low-Voltage Write/High Voltage Read.

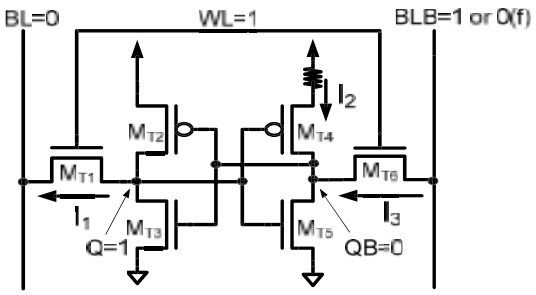


Figure 1: Stability fault in 6-T SRAM cell

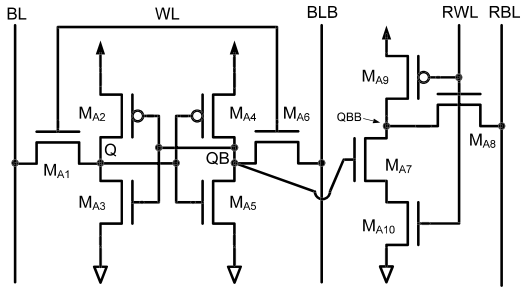


Figure 2: 10-T Sub-Threshold design

Read Equivalent Stress (RES):

In 6T SRAM consecutive read operations are performed to a designated bit-cell in such a way that its word-line kept opened and its data stored by the cross-coupled inverters are constantly attacked by the pre-charged VDD at bit-lines [17], [21]. However, a10-T subthreshold SRAMs utilizes a different read path from its write path and a read operation will turn on only its read word-line but not its write word-line. Such a read operation cannot attack the stored data and detect stability faults. Thus, to apply read equivalent stress technique in 10-T architecture for additional DFT circuit is required to turn on the write word-line and apply floating 1 at write bit-lines with read operation during test mode.

Severe Write:

Here, the write operation is performed by setting BL and BLB line to floating 0 and strong 0 during testing mode rather setting strong 1 and strong 0 at the normal mode. With this type of write operation, successfully writing data becomes more difficult because the floating 0 is opposite to the target value at Q or QB. In presence of open defects on Source/Drain of PMOS transistor weakens the pull-up ability. Hence severe write operation fail to write the correct data and thus the defect can be detected. But this method fails in detecting defects on NMOS transistor. Because, access transistors (MT1 and MT6) cannot pass logic 1 without the degradation especially when operating at low voltages. Therefore, such a severe write operation fail to write data correctly even when there are no defects are present in sub-threshold SRAM. Hence, in order to use this method to detect defect on NMOS transistor it is required to boost the voltage at WL to enhance the ability of passing a value 1 through the nMOS pass transistors during the test mode, again requires extra DFT circuitry to realize.

High-V-Write/Low-V-Read:

This method is also increases the difficulty of a write operation such that the degradation of pull-up or pull-down capability caused by an open defect may fail to write the correct data. At the same time, it is required to make sure that this difficult condition for write will not fail the design without any defect. It means that the low operating voltage for write cannot be too far away from the normal voltage. Also, changing the operating voltage on test equipment takes a significant amount of time.

All the above discussed test methods require additional DFT circuitry which increases the area overhead. In this paper a simple transient (IDDT)current based test method is proposed to unveil various stability faults and effort has been put to localize defects in a memory array. Proposed methodology is presented in next section.

2. Efficiency of I_{DDT} waveform analysis

Open defects (depending on their value) usually may affect the dynamic current consumption in some way. There are five parameters of a waveform that may change in presence of defects as depicted in Figure 2, which include the current waveform width at a given value of current, the charge provided by the waveform, the peak value of the waveform, the time at which the waveform reaches its peak value, and the average value of the waveform.

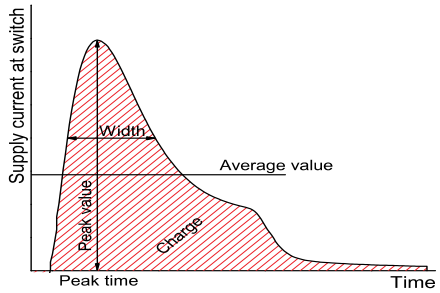


Figure 3: IDDT waveform of fault free 6T-SRAM Cell

3. Proposed methodology for fault detection and localization

1. Fault detection

Test unit contains a memory which stores the current waveform signature of the good circuit response. The current (IDDT) waveform of the memory cell to be tested is sampled at higher rate than the clock period and these samples are used for defect detection and localization. It is observed that for detection of faults, 8 to 10 times over-sampling is required [13], [14]. Even higher sampling rates can also be used to obtain higher resolution in storing the waveform. The fault diagnosis unit compares the response of the good circuit with the observed waveform and if they differ from each other, the circuit is assumed faulty.

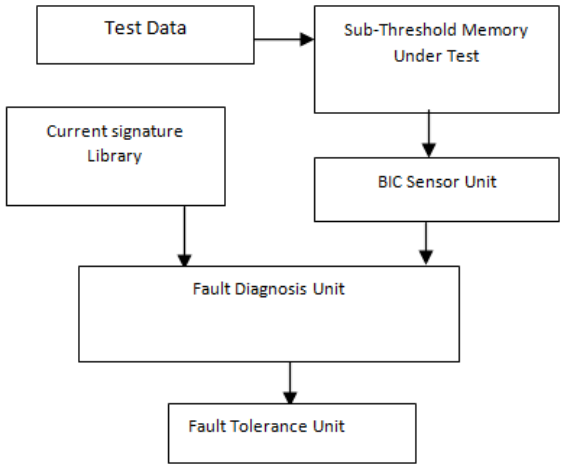


Figure 4: Block diagram of Online Test Unit (OUT)

Fault localization:

Here, the memory is made to operate under two modes: functional or normal mode and test mode. In test mode, all bit lines get disconnected from the cell and data is written on to first cell which will be given as an input to the next cell as shown in fig 3. Thus, each bit-cell in an array is driven by previous cell. Now the data written activates a fault in particular depth and causes abnormal increase in transient current spike of the faulty cell. The time at which the IDDT spike deviates from the good circuit depends on the depth at which the defect resides. The response of good circuit is stored in signature library and the current measurements are made using Built in Current Sensors (BICs). By measuring the delay, Δ, in the response, the degree at which the current waveform of faulty array deviates from that of good cell, the depth at which the fault is located can be known. This information can be used by the Fault tolerance unit which can make decision to replace faulty cell with redundant cell.

4. Experimental Results

In the following experiments, open defect with different resistances on each terminal (gate or source/drain) of each transistor is injected and the minimum resistance which can cause a failure on a read operation or a write operation for Type-A subthreshold SRAM designs is reported. Table 1 lists the minimum detectable resistance of each open defect and the operation which the defect causes a failure (in Column 4). Simulations are carried out at the TT corner and 25C. If the injected defect causes a read failure or write failure, such defect can be easily detected by a conventional SRAM march sequence. It means that, any open defect with resistance lesser than the minimum detectable resistance left undetected during voltage based testing.

The open defects locating on the source/drain of four cross-coupled transistors (M_{A2} to M_{A5}) are highlighted by a gray background color in Table 1. Those defects are classified as a stability fault in Section 3. Opposite to traditional 6T superthreshold SRAMs, no stability faults on the nMOS transistors (M_{A3} and M_{A5}) can be detected, but the stability faults on the pMOS transistors can be detected with a 90 M minimum detectable resistance. This result demonstrates that detecting the stability faults on nMOS transistors is more critical than that on pMOS transistors for Type-A designs. Also, all open defects on the gate of the six transistors (M_{A1} to M_{A6}) have a minimum detectable resistance larger than 390 M, and hence are also relatively hard to detect.

Further, experiments are conducted to reduce the minimum detectable resistance using the test methods discussed in previous section:1) read equivalent stress (RES), 2) severe write, and 3) low-V-write/high-V-read (LVW- HVR). Table 2 reveals that the severe write outperforms the other two test methods by achieving a 6M minimum detectable resistance for pMOS stability faults and a 4.8 M minimum detectable resistance for nMOS stability faults. In addition, the severe write and LVW-HVR can also help to reduce

the minimum detectable resistance at the gate of M_{A1} to M_{A6}, while the other test method cannot. Table 3 shows the corresponding results, in which LVW- HVR achieves a lower minimum detectable resistance at the gate of write pass transistors and pull-up pMOS transistors (M_{A1}, M_{A2}, M_{A4}, and M_{A6}) while the severe write achieves a lower minimum detectable resistance at the gate of pull-down nMOS transistors (M_{A3} and M_{A5}). Overall, severe write is still the most effective test method for 10-T design as it can cover open defects at the most places. Although, severe write method helps in reducing minimum detectable resistance, the range falls in mega-ohms. Hence, any open defect which is less than the minimum detectable resistance recorded in table 2 left undetected and considered as hard-to-find defects.

In order to detect such hard to find defects in the cell an alternative IDDT test method is applied and minimum detectable resistance is reported in column 5. In this method, transient current is monitored and based on the abnormal shoot-up in transient current defects are detected. From table1 it can be found that in later approach minimum detectable resistance is significantly lesser when compared with voltage based testing. Hence along with all hard-to-find faults all weak defects are detectable.

Table 1: Faulty behavior of open defects on 10T-Sub-threshold SRAM

Transistor property Transistor	Transistor name Transistor name	Terminal	Minimum detectable resistance	
			Voltage based	IDDT based
Access	MA1	G	480M(W0 Fail)	1M
		S/D	3.8M(W0 Fail)	100K
	MA6	G	500M(W1 Fail)	100K
		S/D	3.6M(W1 Fail)	100K
Pull up	MA2	G	∞	10K
		S/D	90M(W0 Fail)	60K
	MA4	G	∞	10K
		S/D	90M(W0 Fail)	60K
Pull down	MA3	G	390M (R0 Fail)	1M
		S/D	∞	100K
	M_{A5}	G	390M(R0 Fail)	100K
		S/D	∞	100K
Read pass transistor tran	M_{A8}	G	180M(R0 Fail)	Undetected
		S/D	16.9M(R0 Fail)	Undetected
Read path pull down1	MA7	G	340M(R0 Fail)	Undetected
		S/D	9.1M(R0 Fail)	Undetected
Read path pull down2	MA10	G	240M(R0 Fail)	Undetected
		S/D	6M(R0 Fail)	Undetected
Read path QBB set	MA9	G	2G(R0 Fail)	Undetected
		S/D	∞	Undetected

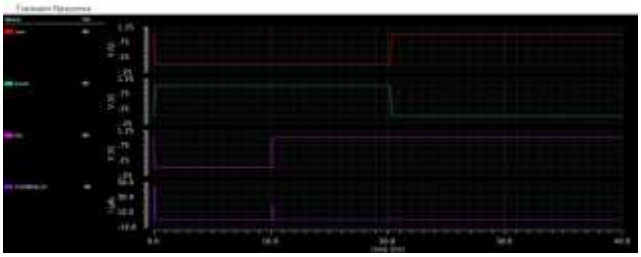
Table 2: Effectiveness of test methods for defect detection at source and drain

Transistor property	Transistor Name	W+R	RES	Severe W	LVH-HVR
Pull-up pMOS	MA2/MA4 S/D	60 MΩ	∞	6.6 MΩ	39.4 MΩ
Pull-down nMOS	MA3/MA5 S/D	∞	790 MΩ	4.3 MΩ	∞

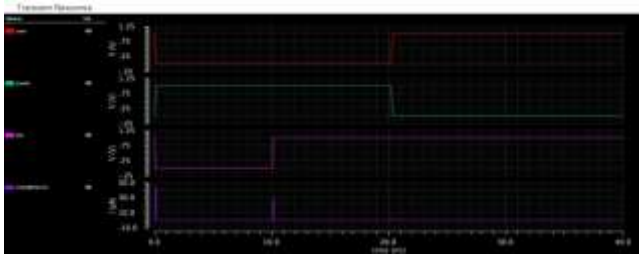
Table 3: Effectiveness of test methods for Gate open defect detection

Transistor property	Transistor Name	W+R	RES	Severe W	LVH-HVR
Write Pass Transistor	MA1(G)	482 MΩ	∞	350 MΩ	32.4 MΩ
	MA6(G)	500 MΩ	∞	420 MΩ	29.9 MΩ
Pull-Up pMOS	MA2(G)	900 MΩ	∞	180 MΩ	60 MΩ
	MA4(G)	800 MΩ	∞	200 MΩ	60 MΩ
Pull-Down nMOS	MA3(G)	370 MΩ	∞	110 MΩ	260 MΩ
	MA5(G)	370 MΩ	∞	230 MΩ	290 MΩ

The measured Iddt waveform of fault free cell and faulty cell with 100KΩ of open defect injected is as shown in Figure 5.Just by correlating the IDDT magnitude of good and faulty cell it is possible to detect the defect but not possible to locate them in an array.



(a)



(b)

Figure 5: Iddt waveforms for (a) fault free (b) cell with 100KΩ open defect at drain of pull-up transistor

To locate the defect in the array one must go for delay based IDDT method in which based on the time at which maximum transient appears depth at which the fault resides can be known.

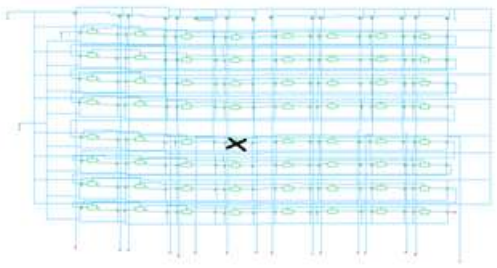


Figure 6: Faulty 8x8 Array

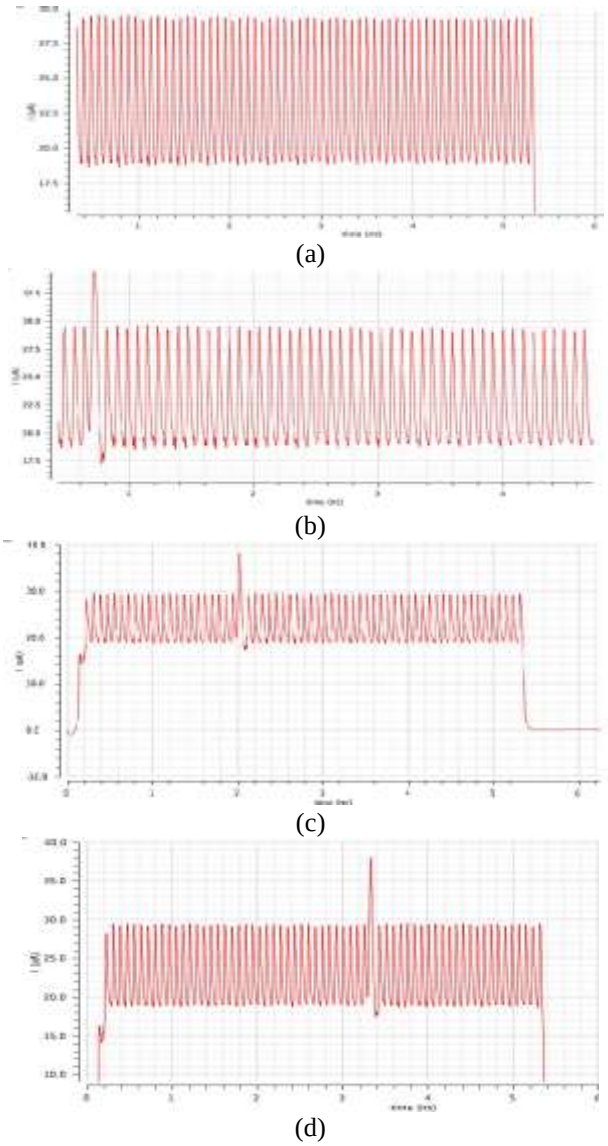
In the experiment, an array of 64-bit sub-threshold memory was built as depicted in Figure 6and circuitry is made to operate under two modes: 1) Functional mode 2) Test mode. During functional mode cell operates normally and in test mode one-bit data is stored to first cell and the same is propagated to next cell to last cell. Thus, the switching activity taking place in each cell results in current spike at IDDT current. It means that an array which has n number of cells causes n number of spikes in IDDT waveform measured at VDD. Thus the total number of spikes at IDDT waveform straightaway indicates number of cells in an array. Figure 7(a) is the IDDT waveform obtained for 64-bit fault free array.

If an applied stimulus activates a fault in a particular depth, the delay in activation of abnormal current manifest itself in the dynamic current waveform. By measuring the delay (Δ), in the response, at which the current waveform of the faulty circuit varies from good circuit, the depth in the array at which the fault resides can be known. The fault can be activated by a signal propagating through previous rows. However, the time measurement in frequency domain requires differentiating the phase response. The measured delay Δ is directly proportional to the number of cells the applied input signal has to pass through before it activates the fault. Clearly, we have obtained delays which increases as the defect move farther from the applied input. Table 4 reports the delay measured by introducing defect at various cells.

Table 4: Efficiency of I_{DDT} Testing Using Various Parameters of the Waveform

Cell Number	Delay (ns)
F18	0.720
F28	2.014
F38	2.314
F48	2.725
F58	3.3885
F68	4.0
F78	4.62
F88	5.27

Figure 7 (b-d) represents IDDT waveform when the defect is injected at 4th, 16th and 40th cell. As discussed earlier abnormal shoot up at 4th, 16th and 40th spike is observed. Thus, the exact location of the fault can be known. Further, the IDDT waveforms are obtained for the array in which multiple cells were faulty. For example, Figure 8(a) represents the I_{DDT} waveform when the array is having fault at cell number 40, 56. With these faults the current.



(a)

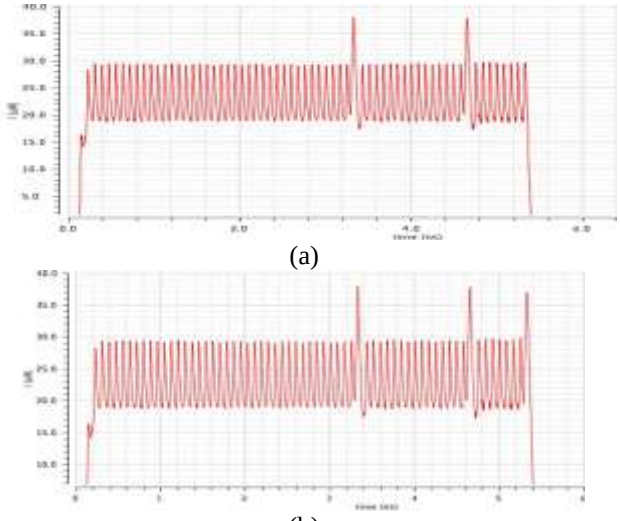
(b)

(c)

(d)

Figure.7: Transient current (I_{DDT}) waveforms for a)Fault free array b) Fault at Gate of MA2/MA4 of 4th cell c) Fault at Gate of MA2 and MA4 of 16th cell d)Fault at Gate of MA2 and MA4 of 40th cell of 40th, 56th spikes are

abnormal in magnitude. Similarly, Figure 8 (b) shows the simulation results drawn in presence of three faults at cell 40, 56 and 64 in an array. Further, shape of the abnormal spike varies from one stability fault to other which helps to locate the fault within a cell. Figure 7(a) and (b) shows the IDDT waveforms when open defect of 100KΩ is injected at 40th cell on Gate and S/D terminals respectively. Figure 9 represents the result window when 64-bit 10T-subthreshold SRAM array having defect at 56th cell. Results are also verified for 1-kb memory.



(a)

(b)

Figure 8: Transient current (I_{DDT}) waveforms with fault at a) 40th and 56th cell b) Fault at 40th,56th and 64th cell

As a part of the work memory array was implemented with various size and results are verified. Figure 9 shows the result window obtained during testing for good and faulty array. Current waveform of the good array was stored. Figure 7 and 8 shows that each spike corresponding to each cell in an array. Average transient current of each spike of the array under the test was compared with that of the corresponding spikes of the good array which is already stored as signature library. If mismatch found, the fault is detected and corresponding cell number is displayed. When the memory array is also tested for multiple cell defects and result window is shown in figure 9.

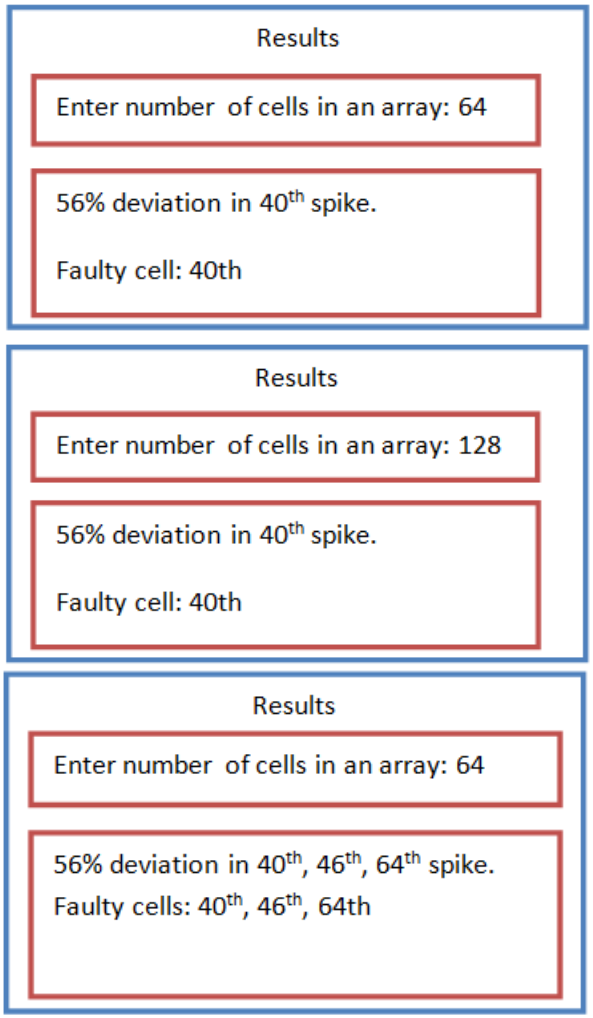


Figure 9: Result window when defects are injected at various cells

5. Conclusion

In this work, the online testing for fault localization in 10T SRAM is investigated using IDDT waveform analysis. we first validated the effectiveness of three different test methods on detecting stability faults through simulation and found that only severe write can cover all stability faults for 10T sub-threshold SRAM design but additional DFT circuitry is required. Moreover, minimum detectable resistance is quite high. Thus any defect with open resistance which is less than the minimum detectable resistances left undetected. It is also found that there is no single test methods which can cover all defects. Proposed method is capable to detect all hard-to-find fault without any additional test circuitry. Another main capability of the transient current based method is its capability in localization of the defects. Here, based on time at which the abnormal transient current, exact position of the faulty cell can be known. In the experiments test is carried out for various processes and found that test efficiency is independent of process variations. It is proved that delay based I_{DDT} analysis is most powerful option for fault detection as well for localization.

References

[1] R.G. Dreslinski, B. Zhai, T. Mudge, D. Blaauw, and

D. Sylvester, "An Energy Efficient Parallel Architecture Using Near Threshold Operation," Proc. Int'l Conf. Parallel Architecture and Compilation Techniques, pp. 175-188, 2007.

[2] [4] R.G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-Threshold Computing: Reclaiming Moore's Law through Energy Efficient Integrated Circuits," Proc. IEEE, vol. 98, no. 2, pp. 253-266, Feb. 2010.

[3] A. Wang, B.H. Calhoun, and A.P. Chandrakasan, Sub-Threshold Design for Ultra Low-Power Systems. Springer, 2006

[4] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "Low-Power Em- bedded SRAM Modules with Expanded Margins for Writing," Proc. IEEE Int'l Solid-State Circuits Conf., vol. 1, pp. 480-611, 2005.

[5] M. Yamaoka, K. Osada, R. Tsuchiya, M. Horiuchi, S. Kimura, and T. Kawahara, "Low Power SRAM Menu for SOC Application Using Yin-Yang-Feedback Memory Cell Technology," Proc. Symp. VLSI Circuits, pp. 288-291, 2004.

[6] B.H. Calhoun and A. Chandrakasan, "A 256kb Sub-Threshold SRAM in 65nm CMOS," Proc. IEEE Int'l Solid-State Circuits Conf., 2006.

[7] T.H. Kim, J. Liu, J. Keane, and C.H. Kim, "A 0.2 V, 480 kb Subthreshold SRAM with 1 k Cells per Bitline for Ultra-Low- Voltage Computing," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 518-529, Feb. 2008.

[8] N. Verma and A.P. Chandrakasan, "A 256 kb 65 nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy," IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 141-149, Jan. 2008.

[9] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "A Variation- Tolerant Sub-200 mV 6-T Subthreshold SRAM," IEEE J. Solid-State Circuits, vol. 43, no. 10, pp. 2338-2348, Oct. 2008.

[10] J. Singh, J. Mathew, D.K. Pradhan, and S.P. Mohanty, "A Subthreshold Single Ended I/O SRAM Cell Design for Nanometer CMOS Technologies," Proc. IEEE Int'l SOC Conf., 2008.

[11] I.J. Chang, J.J. Kim, S.P. Park, and K. Roy, "A 32 kb 10T Sub- Threshold SRAM Array with Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 650-658, Feb. 2009.

[12] M.T. Chang and W. Hwang, "A Fully-Differential Subthreshold SRAM Cell with Auto-Compensation," Proc. IEEE Asia Pacific Conf. Circuits and Systems, 2008