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Design of Self Calibrated DLL Based Clock Generator Using Modified GDI Technique

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Abstract: ***This paper describes a low-jitter delay-locked loop (DLL)-based clock generator for dynamic frequency scaling in the extendable instruction set computing (EISC) processor. The DLL-based clock generator provides the system clock with frequencies of the reference clock, according to the workload of the EISC processor. The proposed self-calibration method and a phase detector with an auxiliary charge pump can effectively reduce the delay mismatch between delay cells in the voltage-controlled delay line and the static phase offset due to the current mismatch in the charge pump, respectively. The self-calibrated output waveform exhibits 9.7 ps of RMS jitter and 73.7 ps of peak-to-peak jitter at 120 MHz. The prototype clock generator implemented in CMOS process occupies an active area of 0.25 µm and consumes power.***

Keywords: Calibration, dynamic frequency scaling (DFS), delay-locked loop (DLL), extendable instruction set computing (EISC).

1. Introduction

The clock generator is generally implemented using a phase-locked loop (PLL) to easily change the output clock frequency. However, PLLs have several weaknesses such as the difficulty of design, high-cost loop filters, and jitter accumulation. Delay-locked loops (DLLs) are a good substitute for PLLs, because they resolve the PLL weaknesses; however, because a DLL uses a delay line instead of an oscillator, its output clock frequency is always the same as its input clock frequency. Therefore, a DLL alone cannot be used as a clock generator.

The extendable instruction set computing (EISC) processor has been used for several portable multimedia applications and Handheld applications usually use a battery as the power source, which stores a limited amount of energy. The limited amount of energy introduces the problem of power constraints. Hence, portable applications should be designed to consume less power to extend the lifetime of the battery.

A dynamic voltage and frequency scaling (DVFS) scheme can support the realization of an energy-efficient embedded processor. Similarly, according to the workload of the EISC processor, a DC-DC buck converter and a delay-locked loop (DLL)-based clock generator can change the supply voltage and the system clock frequency, respectively. By doing so, the EISC processor can be managed to consume energy efficiently. However, embedded processors for mobile applications tend to be exposed to various harsh environments. Especially, supply voltage fluctuations and timing uncertainties caused by process, voltage, and temperature (PVT) variations can significantly degrade the performance of the processor. Thus, the susceptibility of the clock generator to external noises and on-chip variations must be addressed to achieve high performance.

To solve the problem of the previous phase detector and lock detector, a modified GDI based a lock detector is proposed to minimize unnecessary power dissipation. In this paper we proposed a self calibrated clock generator by using modified GDI technique. These technique used to reduce the transistor counts, power dissipation, propogation delay and layout area.

2. Existing Work

The clock generator uses a DLL employing an edge-combining type of frequency multiplication scheme. Since the edge-combiner- based clock generator uses multiphase clocks from the voltage-controlled delay line (VCDL) to produce the output, the delay between the each delay cell in the VCDL should be made equal to achieve an accurate output frequency. However, the PVT variations and device mismatch can cause a delay mismatch in the VCDL, which leads to poor jitter performance of the output clock. Current mismatch in the charge pump results in a static phase offset, which also deteriorates the performance of the clock generator. To reduce the influence of such on-chip variability, novel circuit techniques have been required

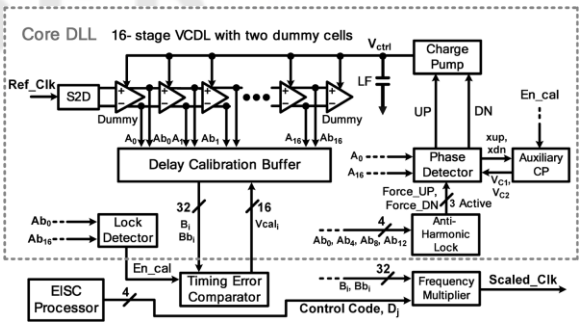

Figure 1: Self Calibrated DLL Based Clock Generator

The entire architecture of the DLL-based clock generator is shown above Fig.1. To take advantage of the fully differential VCDL, a single-to-differential converter (S2D) converts the reference clock into a differential clock. The core DLL was produces 16 pairs of multiphase clocks, which are used for frequency multiplication. The multiphase clocks from the VCDL pass through a self-calibration is consisting of a timing error comparator and a delay calibration buffer.

The lock detector can discern the moment that two input clock edges to the PD are brought into very close alignment. To avoid excessive power consumption, the lock detector enables the delay mismatch calibration and the static phase offset compensation after the core DLL acquires lock. The clock generator uses a 15 MHz clock as the reference clock and gives the EISC processor has a 30MHz clock as the nominal system clock with frequency multiplication of two.

The self-calibration loop consists of a delay calibration buffer and a timing error comparator. The delay calibration buffer consists of 16 separate delay calibration buffer cells shown in Fig. 2 and receives multiphase clocks from the VCDL. Each delay calibration buffer cell consists of a two-stage delay cell with small delay coverage. The schematic of the proposed timing error comparator is shown in Fig. 3(a). Each timing error comparator cell compares three consecutive multiphase clocks from the delay calibration buffer. The timing diagram of the delay calibration buffer is shown in Fig. 3(b). The timing error comparator compares the relative pulse widths of *cal-dn* and *cl-up* , which are the signals indicating the phase difference between adjacent multiphase clocks. Then, it periodically charges or discharges the capacitor, (2.5 pF) according to the pulse widths of *cl-up* and *cl-dn* .

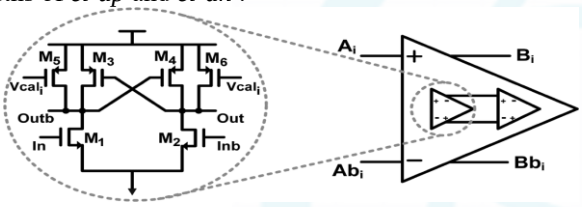

Figure 2: Delay calibration buffer cell

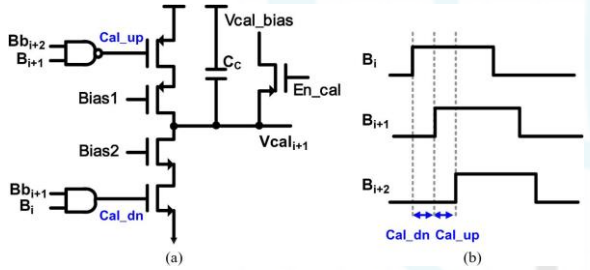

Figure 3: (a) Timing error comparator cell and (b) timing diagram of delay buffer output.

The self calibrated clock generator has more number of transistor counts implement to the lock detector and phase detector. So these disadvantages of poor jitter performance ,occupies large area and low power dissipation.

3. Proposed System

A proposed delay-locked loop (DLL)-based self calibrated clock generator can change the supply voltage and the system clock frequency, respectively. By doing So, the EISC processor can be used to consume energy efficiently. However, embedded processors for mobile applications tends to be exposed to various harsh environments. Especially, supply voltage fluctuations and timing reservations caused by process, voltage, and temperature (PVT) variations can significantly degrade the performance of the processor. Thus, the susceptibility of the clock generator to external noise and on-chip variations must be addressed to achieve high performance.

Depending on the thermometer code from the EISC processor, the frequency multiplier selects and merges short pulses that are generated with the calibrated multiphase clocks. The merged short pulses create a scaled system clock of a desired frequency with a 50% duty cycle through a toggled-pulsed latch. Since multiphase clocks are used for frequency multiplication, an anti-harmonic lock circuit is adopted to prevent the core DLL from locking at more than one reference clock cycle. Without an anti-harmonic lock circuit, the frequency multiplication ratio can be incorrect and can bring about the total failure of clock synthesis. A phase detector (PD) with an auxiliary charge pump reduces the static phase offset, which can cause a spur in the output clock.

The proposed phase detector and lock detector by using modified GDI (gate diffusion input) technique. This technique allows reduce power consumption ,delay and area of digital circuits, while maintaining low complexity of logic design. The method is suitable for design of fast, low power circuits, using reduced number of transistor (as compared to CMOS technique).

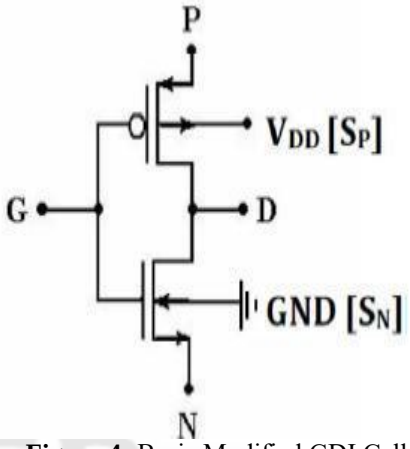

Figure 4: Basic Modified GDI Cell

The Modified-GDI [Mod-GDI] cell contains a low-voltage terminal SP configured to be connected to a high constant voltage (i.e. supply voltage) and a high-voltage terminal SN configured to be connected to a low constant voltage (i.e. Ground). By doing this, the proposed Mod-GDI cell is completely compatible for implementation in a standard CMOS process of fabrication, where bulks of all PMOS transistors are connected to VDD and bulks of all NMOS transistors are connected to GND.

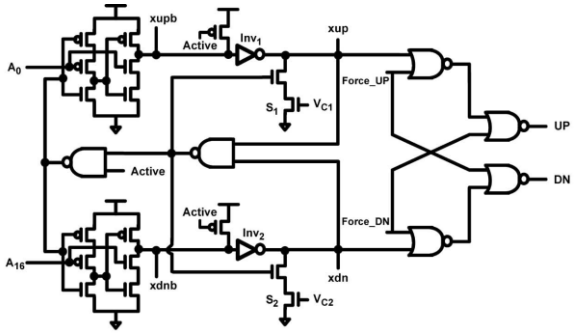

Figure 5: Proposed Block Of Phase Detector

The proposed phase detector incorporating a auxiliary charge pump is shown Fig. 5. After the core DLL is locked, the auxiliary charge pump begins it is operation. The auxiliary charge pump is a simple charge pump that can be generate two control voltages, Vc_1 and Vc_2, using internal UP and DN pulses. Delay mismatch calibration should begin after the core DLL is locked so that the timing error comparator can detect the exact amount of phase error to be calibrated. If the self-calibration circuit operates before the core DLL is locked, the calibration may go in the wrong direction, which would necessitate a lock detection circuit. Static phase offset compensation also needs to be started after locking to detect and adjust the phase error correctly. proposed lock detector measures the delay between the two clocks, Ab_0 and Ab_{16} , from the VCDL. If the measured delay is smaller than the predetermined delay, , the lock detector activates both the delay mismatch calibration and the static phase offset compensation, respectively. Since the timing comparators and the auxiliary charge pump operate only after the core DLL is locked, the initial calibration error and additional power dissipation can be avoided.

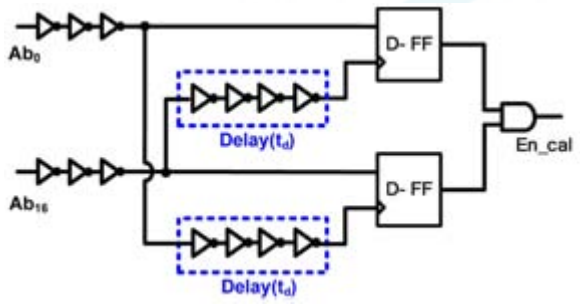

Figure 6: Lock Detector

Finally the architecture of DLL based self calibrated clock generator was implemented in a 0.18µm CMOS process. And these advantages of improve the jitter performance, occupy small area, and low power dissipation.

4. Results

The results produced shown that the method is an efficient one. The self calibrated clock generator is produced and is shown in figure.no.8

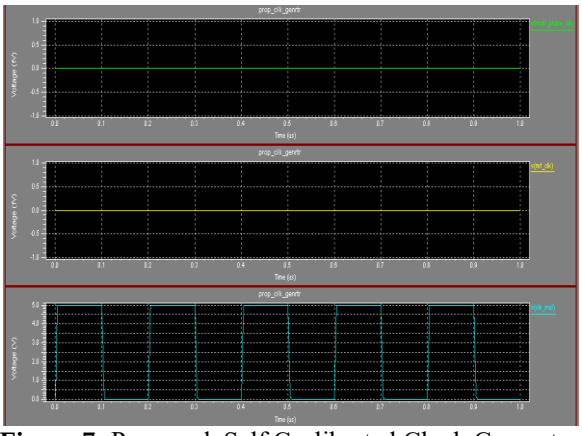

Figure 7: Proposed Self Caclibrated Clock Generator

The proposed modified GDI Techniques consumes less power and reduced propagation delay for low power design of combinatorial digital circuits with minimum number of transistors. The output is shown in fig.no.7

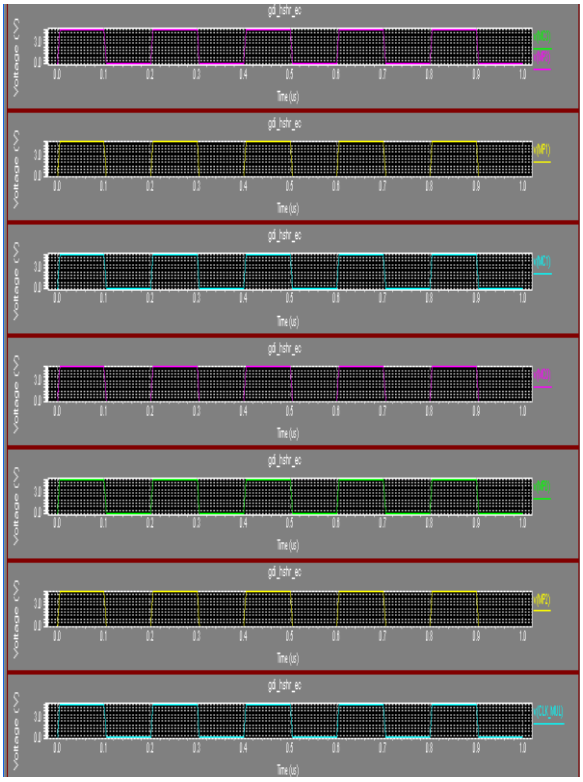

Figure 8: Modified GDI Phase Detector Output

The results are tabulated and shown in table no.1

Table 1: Comparison of Existing and Proposed Design

Designs	Transistor counts	Delay	Power
Existing design	344	6.45235e-010	1.05e-001 watts
Proposed design	292	4.69112e-010	2.65e-002 watts

5. Simulation Results

The simulating results for self calibrated clock generator power and transistor counts are shown in figure 9,10,11, and 12 respectively.

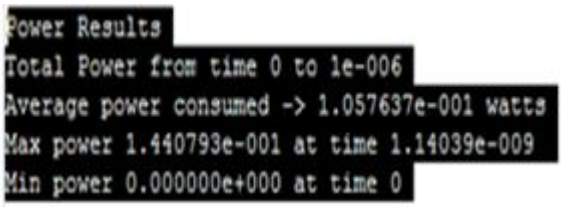

Figure 9: Existing Self Calibrated Clock Generator Power Output.

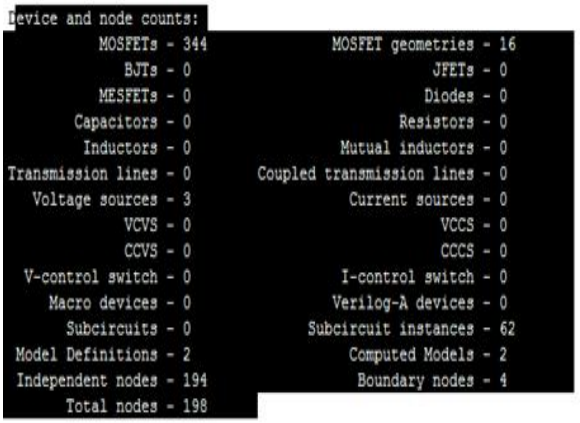

Figure 10: Existing Self Calibrated Clock Generator Transistor Output

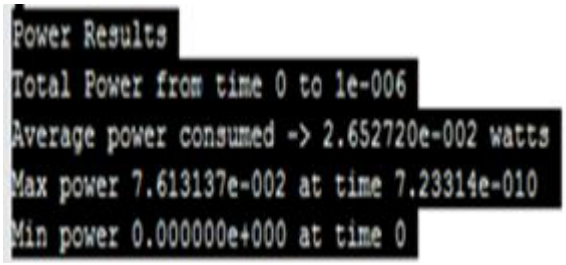

Figure 11: Proposed Self Calibrated Clock Generator Power Output

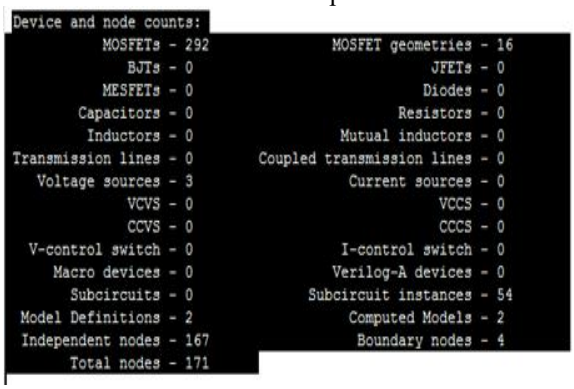

Figure 12; Proposed Self Calibrated Clock Generator Transistor Output

6. Conclusion

The proposed self-calibrated DLL-based clock generator occupies the smallest active area among those with a self-calibration circuit and exhibits excellent jitter performance.. The clock generator can produce an output clock that varies its frequency according to the workload of the EISC processor. The DLL based self calibrated clock generator in phase detector and lock detector by using modified GDI technique. These technique are used to reduce power, area, delay for the circuits. The proposed DLL based clock generator is implemented in a 0.18µm CMOS technology and the measured power consumption to frequency ratio is only 2.9 mw/mhz. so it can be used in portable mobile applications and microprocessors.

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