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Design of FIR Filter Architecture using Various Efficient Multipliers

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Abstract: ***Finite impulse response (FIR) filter is one of the important components in any DSP and communication systems. The output from the DSP processor is depends on the FIR filter, so need an efficient FIR filter design, to achieve an efficient output. Filter architecture contains many components; one of the main components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters. In the existing Wallace tree multiplier was designed and implemented using verilog HDL. This multiplier needs many gates to implement the design. So it takes more area and delay. To reduce the drawbacks in the existing system, to propose a new efficient multiplier named as Birecoder multiplier. It is one of the best multiplier in the digital circuit design. This multiplier overcomes the existing multiplier drawbacks. Multiplier is design by verilog HDL, after the design Wallace tree multiplier is compared with Birecoder, and analyzes the performance of the multiplier. Implement the design using Modelsim 6.3c and Xilinx ISE. Finally the designed multipliers are applied into the FIR filter, and show the best filter.***

Keywords: Wallace tree, Birecoder, Modelsim 6.3c, Xilinx ISE, FIR filter

1. Introduction

One of the most extensively used functions executed in DSP is Finite Impulse Response (FIR) filtering. In several applications, in order to attain high spectral suppression and noise reduction, FIR filters are used. A lot of prior efforts for decreasing power consumption of FIR filter usually focus on the miniaturization of the filter coefficients whereas maintaining a fixed filter order. FIR filter structures are simplified to minimizing the number additions, subtractions and add & shift operations [1]. Though, one of the problems encountered is that one time the filter architecture is determined, the coefficients cannot be altered; consequently, those are not appropriate to FIR filter with programmable coefficients [2].

Finite impulse response (FIR) filter is one of the important components in any DSP and communication systems [3]. The output from the DSP processor is depends on the FIR filter, so need an efficient FIR filter design, to achieve an efficient output. Filter architecture contains many components; one of the main components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters. In this project, the existing Wallace tree multiplier was designed and implemented using verilog HDL [4-8]. This multiplier needs many gates to implement the design. So it takes more area and delay. To reduce the drawbacks in the existing system, to propose a new efficient multiplier named as Birecoder multiplier. It is one of the best multiplier in the digital circuit design. This multiplier overcomes the existing multiplier drawbacks. Multiplier is design by verilog HDL, after the design Wallace tree multiplier is compared with Birecoder, and analyzes the performance of the multiplier [9-11]. Implement the design using Modelsim 6.3c and Xilinx ISE. Finally the designed multipliers are applied into the FIR filter, and show the best filter. Finite Impulse Response (FIR) filter is used to filter the noise or unwanted signals at finite impulse durations. Multiplication and Accumulation (MAC) unit estimates the duration of periodic impulses [12].

Therefore, high performance of multiplication and accumulation architectures is required to improve the performance of digital FIR filter [13]. In this paper, a novel, reduced complexity SQRT CSLA based Bi-Recoder multiplier is incorporated into multiplication of direct form FIR filter. Hence, absolutely we can improve the performance of digital FIR filter than other best existing FIR filters [14].

Very Large Scale Integration

Very Large Scale Integration (VLSI) is the process integrating thousands of transistors into a single chip. The major concerns of the VLSI design were area, performance and power. In the past, the designers were directed towards increasing the speed of the digital system; hence the present day technologies posses computing capabilities that make possible personal work stations, sophisticated computer graphics and multi-media capabilities such as real time speech recognition and real time video. Another significant change in the attitude of the users is the desire to have access to this computation at any location, without the need to be physically tethered to a wired network. The requirement of portability thus places severe restriction on size, weight and power. This Technology not only helped to reduce the size of the devices but also improved their speed. In a large IC the components are so small and close together that capacitance is much smaller and, thus less power.

Digital Signal Processing

Digital signal processing (DSP) is the use of digital processing, such as by computers, to perform a wide variety of signal processing operations. The signals processed in this manner are a sequence of numbers that represent samples of a continuous variable in a domain such as time, space, or frequency.

Digital signal processing and analog signal processing are subfields of signal processing. DSP applications include audio and speech signal processing, sonar, radar and other sensor array processing, spectral estimation, statistical signal processing, digital image processing, signal processing for telecommunications, control of systems, biomedical engineering, sesmic data processing, among others.

2. Prior Work

Multipliers play an important role in today's digital signal processing and various other applications. The existing method uses Wallace multiplier technique. A Wallace tree is an efficient hardware implementation of a digital circuit that is used to multiply the two integers.

The Wallace tree has three steps:

- Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding results. Depending on position of the multiplied bits, the wires carry different weights.
- Group the wires in two numbers, and add them with a conventional adder.

The block diagram for the existing methodology with its functionality is shown below in the figure 1.

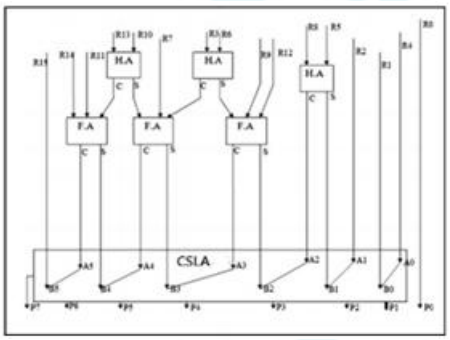

Figure 1: Wallace tree multiplier

a, structure of reduced complexity wallace multiplier

Wallace multiplier uses full adders and half adders to reduce the partial product tree to two rows, and then a final adder is used to add these two rows of partial products. The final adder that is used in the Wallace tree multiplier is Carry select adder the diagram of reduction of wallace tree is show below in the figure 2.

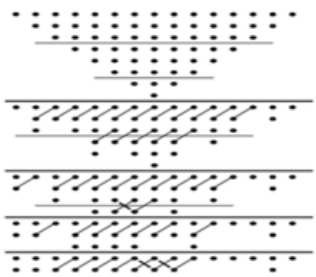

Figure 2: Example of Wallace tree reduction

The carry select adder generally consists of two stages of Ripple carry adder. Adding two n-bit numbers with the carry select adder is done with two adders(therefore two ripple carry adders)in order to perform the calculation twice, one time with the assumption of carry being one and the other with zeros and finally added with a multiplexer. Due to this the computations increase. If the no of bit size increase the propagation delay also become large. Hence, it occupies large area for computation.

In order to overcome this problem, Wallace multiplier with proposed SQRT CSLA is designed.

3. Proposed Work

The proposed structure uses the Multiply and Accumulate (MAC) bi-recoder multiplier. And the final stage of the addition is done by Square Root Carry Select adder. In order to overcome the disadvantages of the existing method, such that the Area (LUT and Slice) ,delay Finite Impulse Response (FIR) filter is used to filter the noise/unwanted signals at finite impulse durations. Multiplication and Accumulation (MAC) unit estimates the duration of periodic impulses. Therefore, high performance of multiplication and accumulation architectures is required to improve the performance of digital FIR filter.

a, Bi-recoder multiplier

The partial product generation is the first method of any multiplier According to array multiplier with the proposed structure is shown below in the figure 3. The AND gates are used to provide partial product generation. On the other hand, 2:1 Multiplexers are used to provide partial product generation. Multiplicand value is directly given to one of the input of 2:1Multiplexer and N-bit of zero's are given to another input of 2:1 Multiplexer.

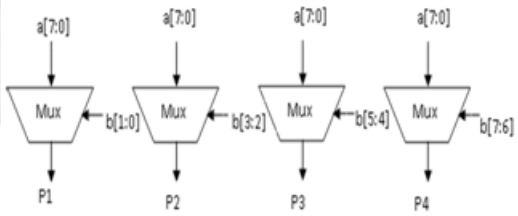

Figure 3: Bi-Recoder Multiplier

For instance, 8-bit multiplier requires 8 multiplexer to provide the partial product results. In every stage, single bit of multiplier is considered as selection input of Multiplexer. If it is zero, Multiplexer simply passes '0' to output else if it is one, Multiplexer passes the multiplicand value to output. Multiplexer based partial product generation technique considered as a basement tutorial for designing a novel Bi-Recoder multiplier. In every stage of Bi-Recoder multiplier, two bits of multiplier value are considered as selection input. If it is '00' means, Multiplexer simply passes'0' to output else if it is '01' means, Multiplexer passes the multiplicand value to output else if it is '10' means, Multiplexer passes the 1-bit left shifted value of multiplicand to output else it is '11'

means, Multiplexer passes the addition value of multiplicand and 1-bit left shifted value of multiplicand to output. In this way, Bi-Recoder multiplier produces the partial product values effective.

b, Bi-recoder based fir filter

Digital Signal Processing (DSP) operations are widely used in wireless communication Technologies to control and guide the signal flows. Convolution, Correlation, Frequency Transformation and filtering are the important operations of DSP applications. In this research work, Finite Impulse Response (FIR) filter is considered for improving the performance of digital filtering process in wireless communication technology. Large endeavours have been worked on direct form digital FIR filter to improve the performance in terms of high speed and throughput. The relationship of input- output of Linear Time Invariant (LTI) System is represented as in equation,

$$yout(n) = \sum Coeff\ p\ Xin\ (n - 1)$$

Where, xin(n) represents the input samples of FIR filter, yout(n) represents the output samples of FIR filter, N is the order of the filter or length of the filter and Coeff p denotes the coefficient of filters. Impulse response of FIR filter must be finite and therefore, Periodical multiplication and accumulation structures are used to maintain the impulse response of FIR filter as finite. Square Root Carry Select Adder (SQRT CSLA) is one of the best VLSI based adders, because it utilizes less hardware complexity and high speed. The combination of Ripple Carry Adder (RCA) and Binary to Excess1 Conversion (BEC) unit is to reduce the propagation delay of addition process. In SQRT CSLA, N-bit data can be divided into √N groups for performing parallel addition process. Reduced complexity Wallace multiplier is developed for the design of digital FIR filter. The matrix of triangular order outputs are divided into three row groups. Full Adders (FAs) are used for adding three bits and Single bit and a group of two bits are moved to the next stage directly. In final stage of Wallace tree multiplier require sufficient N-bit binary adder for performing accumulation operation. Efficient CSLA circuit is used for addition part of reduced complexity Wallace multiplier. Parallel Prefix Han-Carlson Adder, for addition part of reduced complexity Wallace multiplier.

Also both reduced complexity Wallace multiplier and CSLA circuits are incorporated into digital FIR filter. Different types of multipliers are used in various literatures to design FIR filter. Similarly, Multiple Constant Multiplication (MCM) technique for multiplication part of digital FIR filter. In this, design of FIR filter is done by using Verilog Hardware Description Language (Verilog HDL) of digital FIR filter, a novel Bi-Recoder Multiplier and reduced complexity SQRT CSLA are developed in this research work. Large endeavors have been worked on direct form digital FIR filter to improve the performance in terms of high speed and throughput.

c, square root carry select adder (sqrtcsla)

The proposed structure consists of SQRT CLSA is shown in figure 3.4.

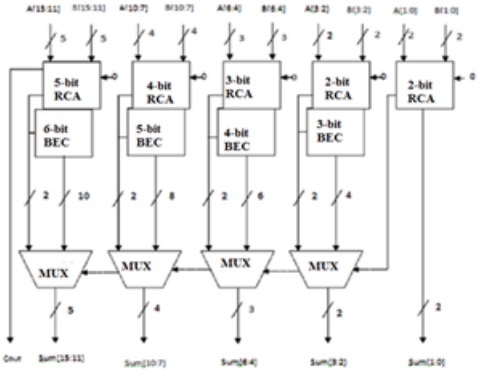

Figure 4: SQRT CSLA

Ripple Carry Adder (RCA) is one of the basic VLSI based adders which is largely affected by Carry Propagation Delay (CPD). To reduce the CPD of circuit, Carry Select Adder (CSLA) is developed in past. In CSLA circuit, N-bit data is divided into √N groups to provide the parallelism. Hence, this circuit is named as SQRT CSLA. Divided each and every group can operate instantly at same time. However, RCA circuits of SQRT CSLA reduce the performance in terms of speed. Hence, one set of RCA circuits is replaced by BEC circuits (have same functionality with less number of gates) to increase the speed of the adder significantly. The circuit diagram of 16-bit BEC based SQRT CSLA circuit is illustrated in the figure 5.

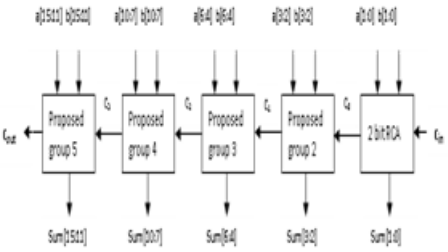

Figure 5: Proposed SQRT Carry Select Adder

Every group structures have RCA, BEC and Multiplexer circuits, hence most essential components to design group structures of SQRT CSLA are Full Adders (FAs), Half Adders (HAs), Logic Gates (AND, EX-OR and NOT) and Multiplexers. For instance, group-2 and group-3 structures of 16-bit SQRT CSLA circuits are illustrated. In this structures, combination of FA and HA gives the results of RCA and it is followed by BEC circuit which indicated in dotted line of fig.4.3.1. Finally, Multiplexors are used to provide final sum outputs. Carry input (Cin) is given to the selection input of first group of Multiplexers. Remaining groups get the Carry inputs from previous groups. Hence, final stage of SQRT CSLA only cause little CPD than traditional RCA circuit is shown in the figure 6.

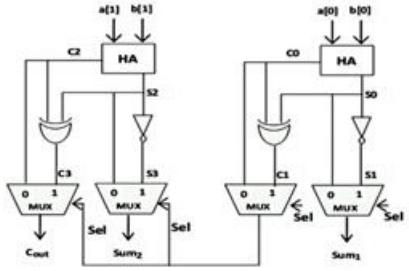

Figure 6: Proposed Group2 structure for proposed SQRT CSLA

In this, the complexity of BEC circuits and multiplexer circuits are realized and re-constructed to increase the performance in terms silicon area and power consumption. Redundant logic function of each group structures are identified and eliminated to reduce the hardware complexity. Hence, the developed adder circuit is named as "Reduced Complexity SQRT CSLA. The circuit diagram of reduced complexity SQRT CSLA for 4-bit addition similarly, we can extend and compress the circuit of for group-5 structure and group-2, group- 3 structures. Theoretically, 38% of gate counts are reduced in reduced complexity SQRT CSLA than traditional SQRT CSLA adder circuits. Further, the performance of reduced complexity SQRT CSLA is compared with Compressor based adder circuits is shown in the figure 7.

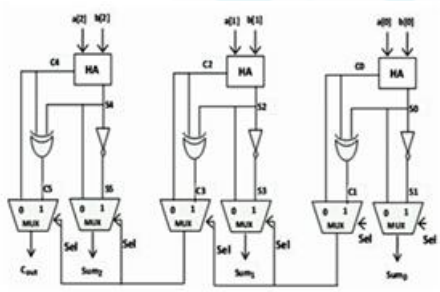

Figure 7: Proposed Group3 structure for proposed SQRT CSLA

Both compressors based digital adder and reduced complexity SQRT CSLA adder is incorporated into the addition part of Bi-Recoder multiplier independently. The performance of reduced complexity SQRT CSLA based Bi-Recoder is better than the performance of compressors adder based Bi-Recoder due to less hardware complexity of reduced complexity SQRT CSLA. Both compressors based digital adder and reduced complexity SQRT CSLA adder is incorporate addition part of Bi-Recoder multiplier independently. The performance of reduced complexity SQRT CSLA based Bi-Recoder is better than the performance of reduced complexity SQRT CSLA. Hence, this circuit is named as SQRT CSLA. Divided each and every group can operate instantly at same time. Therefore the resultant partial products of the bi-recoder multiplier.

4. Results and Discussions

a, Simulation output of Bi-recoder multiplier

The overall performance of the Bi-recoder multiplier and the simulation output is shown in the figure 8.

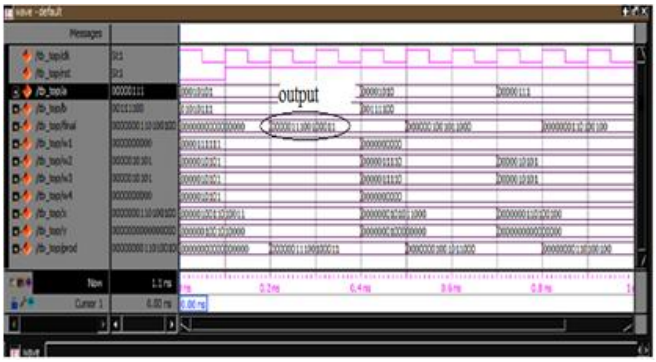

Figure 8: Simulation output of Bi-recoder multiplier

b, Comparison between the result

The comparison between the existing Wallace tree multiplier and the proposed Bi-recoder multiplier is shows the delay, area, power in the figure 9.

Comparison between the results

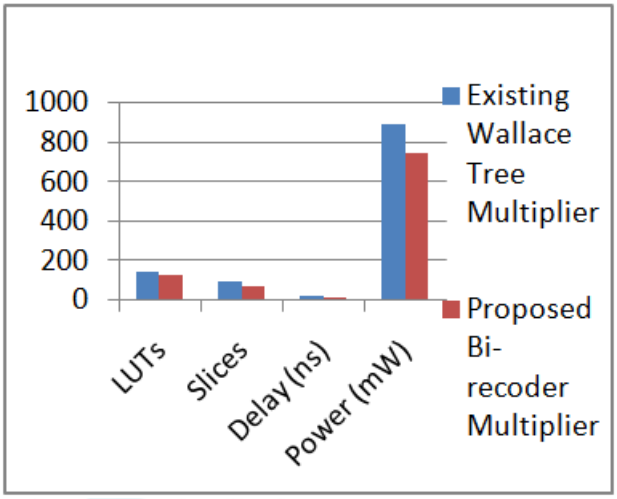

Figure 10: Overall manual Outputs

5. Conclusion and Future Enhancement

a, Conclusion

This project presents a Bi-Recoder multiplier with help of multiplexer. This reduces N rows of partial products into N/2 rows of partial products with slight increase in bit-lengths. Due to lesser number of partial products, the number of adders used to make partial product addition is also less. It reduces slices by 6% and LUT by 7% compared to Wallace tree multiplier. Power consumption of Bi-Recoder multiplier reduces up to 60% than Wallace tree multiplier.

Tabulated parameter area, power and delay:

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	130	3,840	3%	
Logic Distribution				
Number of occupied Slices	72	1,920	3%	
Number of Slices containing only related logic	72	72	100%	
Number of Slices containing unrelated logic	0	72	0%	
Total Number of 4 input LUTs	130	3,840	3%	
Number of bonded IOBs	34	141	24%	
IOB Flip Flops	16			
Number of BUFG/BUFGMUXs	1	8	12%	

Tabulated area

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.084	1	--	--
Logic	0.001	130	3840	3.4
Signals	0.004	128	--	--
IOs	0.494	34	141	24.1
Total Quiescent Power	0.043			
Total Dynamic Power	0.702			
Total Power	0.746			

Tabulated power

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Timing Summary:
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Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: 20.165ns
   Maximum output required time after clock: 6.216ns
   Maximum combinational path delay: No path found

Timing Detail:
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All values displayed in nanoseconds (ns)
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Tabulated delay

b, Future Enhancement

The drawback of the birecoder multiplier is the slight increase in the bit- length therefore in the future it can be implemented by using the Russian peasant multiplier which is mainly used to reduce the bit length.

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