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Design of CMOS Current Comparator FVF with VF Level Shifter using for Low Power Applications

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Abstract: ***A new method is discovered by a flipped voltage follower with voltage follower level shifter (LSFVF) is comparator input stage. The CMOS current comparator design reduces power consumption and improves speed of the performance. The conventional current comparator is used for high speed response and low voltage. The comparators are compared in terms of parameters like delay, power dissipation, number of transistors used. The Circuit simulations were performed in CMOS 130nm technology.***

Keywords: Current comparators; current mode circuits; FVF; Analog integrated circuits

1. Introduction

The current comparator [1] plays an important role in analog circuit design for current mode circuits, which is used to compare the two current signals. A fundamental component of current comparator used to analog systems, i.e. analog to digital converters (ADC'S), frequency converters etc. The comparators have particularly used in signal processing applications and data converters. The current comparator is need for reduce power consumption and increase the speed in VLSI circuits [3]. The current comparator proposed by`[4] traff's circuit shown in figure.1(a),voltage follower used as comparator input stage i.e. M1 and M2 transistors and M3 and M4 transistors used CMOS inverting stage amplifiers. The difference of two input currents I_{in}andV_{out} represents compared result between input current to output voltage. The input stage M1 and M2 transistors are turned off at this time increasing the input resistance, whenever the input current is low, and the current comparator dynamic response time increased.

Figure 1(b) the M5 and M6 transistors used to reduce the dead band region by using level shifters and the response time also reduced. However this current comparator circuit adding two biasing current sources, so the power consumption increased. A continuous time current comparator is used for low power applications and shorter delay time. The current comparator proposed by [7] MR transistor added to the resistive feedback network to the NMOS transistor to reduce the input resistance. The proposed current comparator [8] one drawback the number of transistors increased and also increase more power consumption and propagation delay.

2. Proposed Current Comparator

1. Comparator Design

The schematic diagram of proposed current comparator circuit is shown in figure 1. This circuit consists of CMOS inverter, FVF with voltage follower level shifter (LSFVF) and input current, power supply. Here FVF with VF level shifter is used low power consumption and delay.

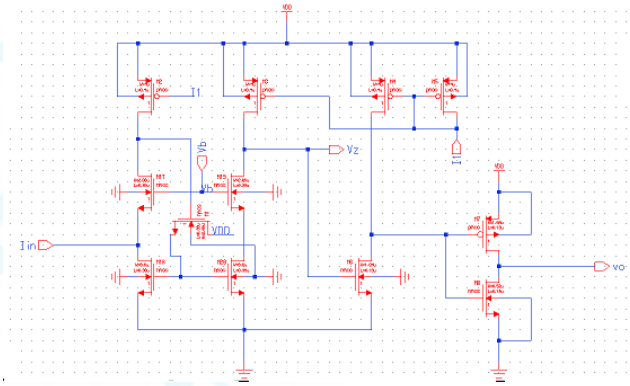

Figure 1: Proposed CMOS current comparator

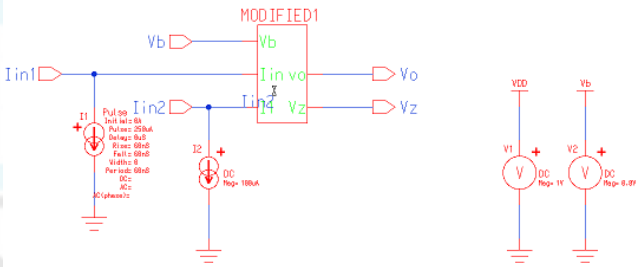

Figure 2: Simulation of proposed current comparator

2. FVF with VF Level Shifter (LSFVF)

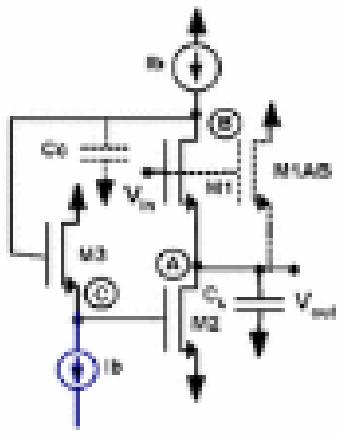

Figure 3: FVF with VF level shifter

The voltage follower is one of the basic building block of analog circuits, a gate source voltage of M1 transistor biased on the source side, with a constant current source I_b.

The key element FVF is replaced by FVF with voltage follower level shifter (LSFVF) is used, the level shifter include transistors M1 and M2 is drain and gate terminals. The proposed current comparator is used FVF with voltage follower level shifter (LSFVF) is large output voltage compared to the conventional current comparator.

$$I_{ref} = \frac{\text{current input range}}{2^{n-1}}$$

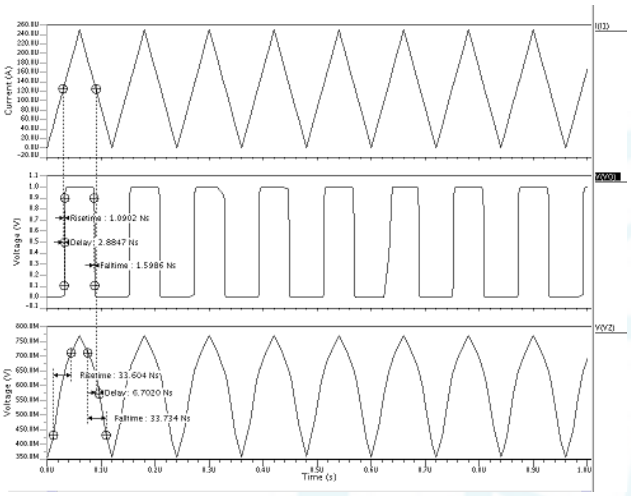

Figure 4: Proposed comparator simulation results

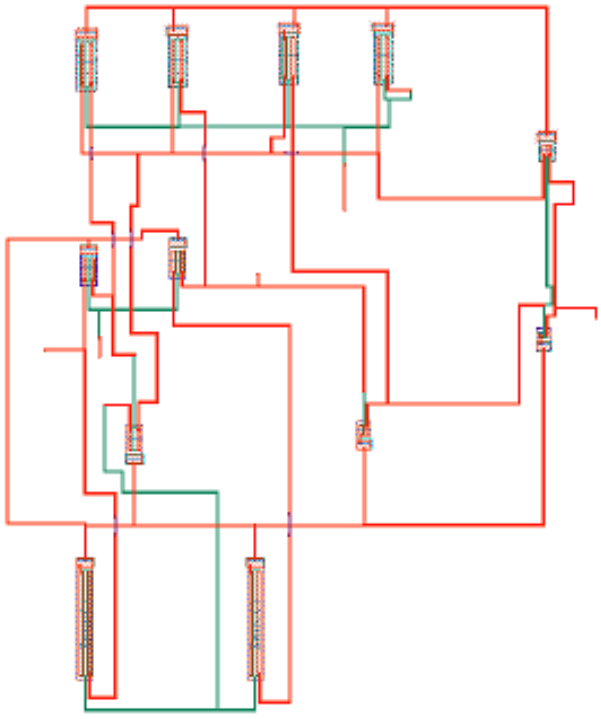

Figure 5: Proposed current comparator layout in 130 nm technology

The current comparator implementation flipped voltage follower with an NMOS inputs differencing two currents i.e. input current I_{in} and reference current I_{ref}, one output voltage V_o.

3. Current Mode Flash ADC

An application of a3- bit current mode flash ADC is implemented as shown in figure 6. Where input current represents I_{in} represents and reference current represents I_{ref}.The current comparator to be employed for 3-bit conversion is given by 7 inputs. The current comparators consist of two currents, one is input current and another one is reference current. Each comparator input current I_{in} compares with its successive reference current I_{ref}, hence all the current comparators comparison in parallel, so this structure is also called as a parallel analog to digital converter (ADC). The comparator output converted into thermometer code to corresponding binary code by a7×3 encoder blocks. The comparator inputs are C7 (MSB) toC1 (LSB), the encoder outputs are B2 (MSB) to1 B0 (LSB), respectively.

The 7×3CMOS encoder, shown in below Figure.7, has been designed for thermometer to binary conversion which remains the same for these entire current modes flash ADC's.

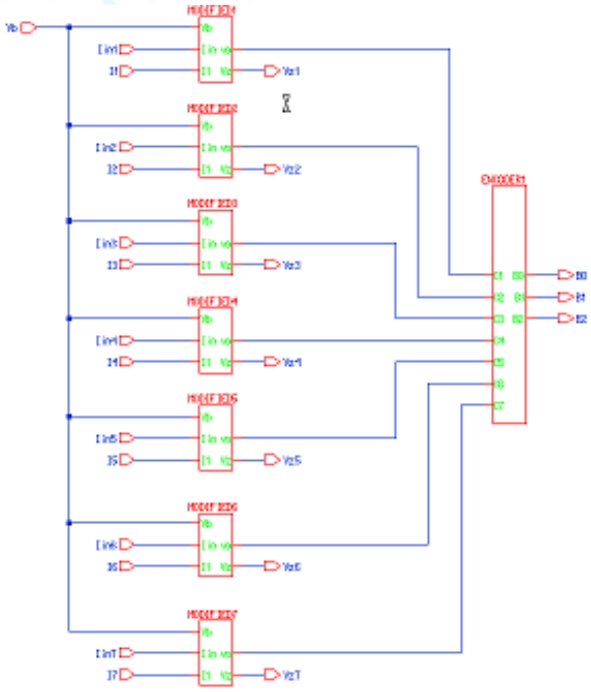

Figure 6.3-Bit Current mode Flash ADC

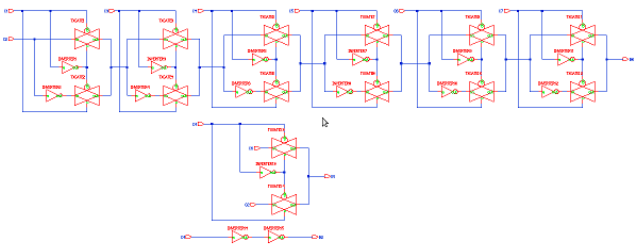

Figure 7: 7*3 CMOS encoder

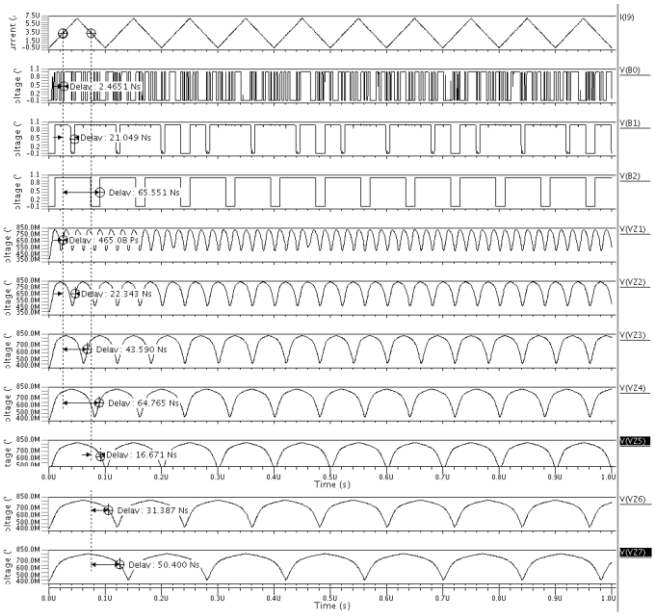

Figure 8: Pre layout simulation results of cm flash ADC

3. Simulation Results

The FVF with VF level shifter circuit is simulated using 130nm CMOS technology. Here 1V (Vdd) supply voltage is taken for both pre layout and post layout simulation. The FVF with VF level shifter circuit offers less propagation delay, less power consumption and also this circuit provides 2.88ns and 278.25uw at input current pulse of 250uA.

4. Conclusion

Here the current comparator is employing by using FVF with VF level shifter as an input stage has been proposed. In this current comparator low power and high speed applications. The comparator simulation results are improved performance and can be used in analog to digital converters.

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