International Journal of Scientific Engineering and Research (IJSER)
ISSN (Online): 2347-3878
Index Copernicus Value (2015): 56.67 | Impact Factor (2017): 5.156

Application of 6:2 Compressor in the Design of Multiplier

Arthi R[1], Dr Senthilkumar B[2], Gowrishankar R[3], Tamilselvan S[4], Dr. Sathish Kumar N[5]

[1]Assistant Professor, KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore – 641 402, India
arthi.r04[at]gmail.com
[2]Professor, KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore – 641 402, India
senthilkit2016[at]gmail.com

[3]Associate Professor, KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore – 641 402, India
rgowri2017[at]gmail.com
[4]Assistant Professor, KIT-Kalaignarkarunanidhi Institute of Technology, Coimbatore – 641 402, India
tamilselvanece87[at]gmail.com
[5]Professor, Sri Ramakrishna Engineering College, Coimbatore – 641 022, India
nsk20022002[at]gmail.com

Abstract: ***Multiplier is the key element in the digital and high performance systems like FIR filters, processors and controllers. Multipliers are complex units and play an important role in deciding the overall area, speed and power consumption of digital circuit design. Hence, the design of multiplier must utilise the less number of transistors. Full adder is used to design such multiplier. Here the utilisation of number of adders has been reduced by introducing different compressor methods. The result achieved with 40% reduction in area, 05% reduction in power, 45% reduction in delay and 40% reduction in number of transistors.***

Keywords: Multiplier, full adders, Area, Power, Compressor

1. Introduction

The power consumption, delay and area are always been an important design considerations for any chip design. Many processor structures incorporate multipliers in its design. Delay of the circuit inevitably changes with the delay of the multiplier. Therefore research is going on to reduce the delay of multiplier so that the delay of whole circuit can be reduced. Wallace tree multipliers are quite fast among the available multipliers and they used carry save addition algorithm. However the speed of operation of multiplier is still a tough task to achieve.

The Wallace tree multiplier involves ANDing of multiplier and multiplicand bits for the generation of partial products. In second phase half adders and full adders has been used for the reduction of generated partial products in two rows. The basic process of multiplication involves three essential steps [5] that are generation of partial products, reduction of the partial products and summation of the reduced partial products in order to produce the final product.

The overall delay of the multiplication process may be reduced by applying delay-reduction techniques in any or all of the three stages [6]. For high speed multiplication, compressors have been considered as the most efficient building blocks. Rather than entirely summoning partial products with the help of carry save adder/Ripple adder tree in the compressor technique the partial products in a single column are together reduced. This would complete the same task in lesser time, efficiently controlling power dissipation and optimization of the area.

2. Traditional Wallace Tree Multiplier with Existing Full Adder

Wallace proposed the column compression technique for fast multiplication operations in which the total delay is proportional to the logarithm of the word length of multiplier operand [1].

The Wallace tree multiplier with column compression technique is faster than array multipliers, because the delay in an array multiplier varies linearly, whereas in Wallace it varies logarithmically [4]. The existing Wallace tree Multiplier uses full adder given in figure 1.

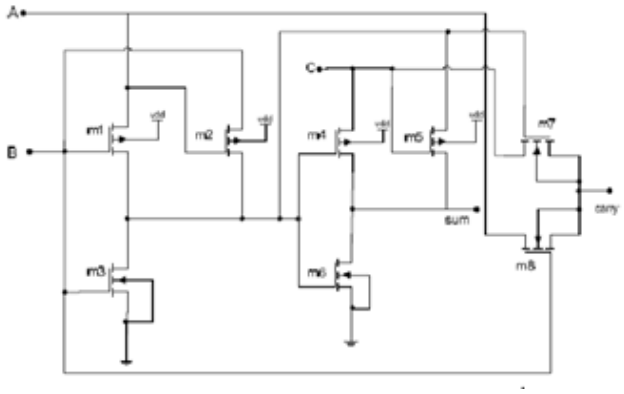

Figure 1: Existing full adder

The existing Wallace tree multiplier is faster than array multiplier but it comes with a disadvantage of layout complexity. By decreasing the number of adders in the partial product reduction stage [2], the latency in the Wallace tree multiplier can be reduced. To overcome this drawback compressor technique has been introduced in this work.

3. Traditional Wallace Tree Multiplier with Proposed Full Adder

The proposed modified full adder circuit as shown in figure 2.

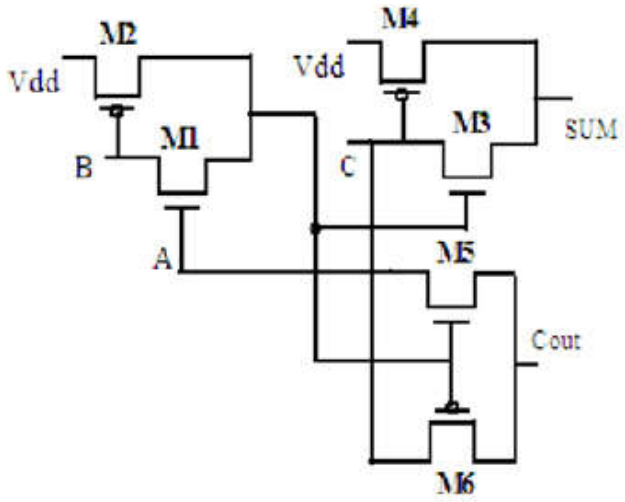

Figure 2: Proposed full adder

The number of transistors reduced in the structure of full adder in order to reduce latency, area and power consumption.

Sum=(BXORC)'A+(BXORC)A' (1)
Carry=B(BXORC)+A(BXORC) (2)

The modified expression of sum for full adder is given in equation (1) and the modified expression of carry is given in equation (2).

3.1 Compressor Based Wallace Tree Multiplier

4:2 compressors were introduced by Weinberger, which consists of five inputs and three outputs shown in figure 3.

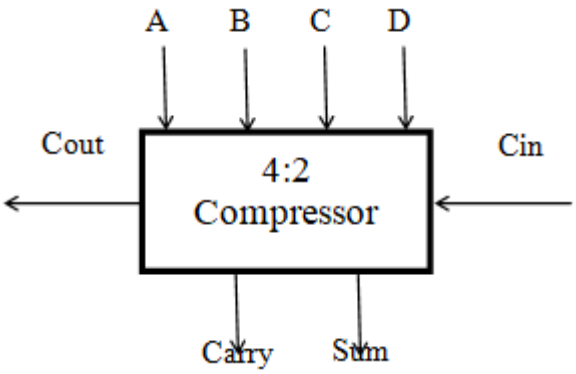

Figure 3: 4:2 Compressor

It compresses four partial products into two, thus offering a higher compression ratio and a more regular interconnection structure than its 3:2 counterparts. The input-output relationship of the compressor is given in equation (3)

x1 + x2 + x3 + x4 + cin = sum +2*Cout+ 2* Carry (3)

4:2 compressor is designed by intricate connection of two 3:2 compressor. The structure has a delay of four XORs and its notable feature is that it is free from carry. The carry from the previous stage is not propagated to the next stage.

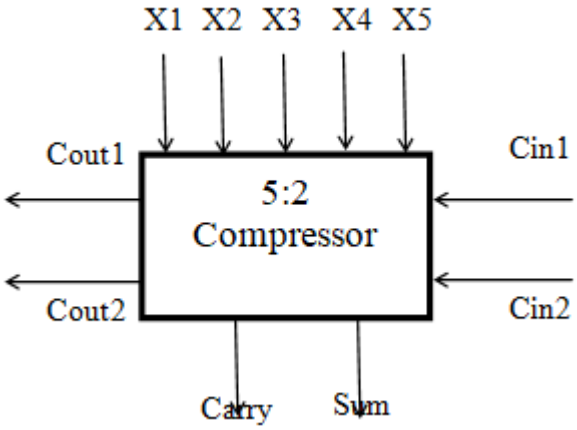

Figure 4: 5:2 Compressor

5:2 is the third widely used compressor. Its block diagram is shown in figure 4. It consists of seven inputs out of which five are direct inputs and two are carry-in bits from previous stage [3]. Similarly, there are four outputs of which two are carry-out bits to the next stage and the other two are sum and carry bits. 5:2 compressors can be designed by cascading three 3:2 compressors. The input-output relationship is governed by following equation (4)

x1 + x2 + x3 + x4 + x5 + cin1 + cin2 = sum + 2(carry+cout1 +cout2) (4)

similar to the above design, the 6:2 compressor has been designed and is shown in figure 5.

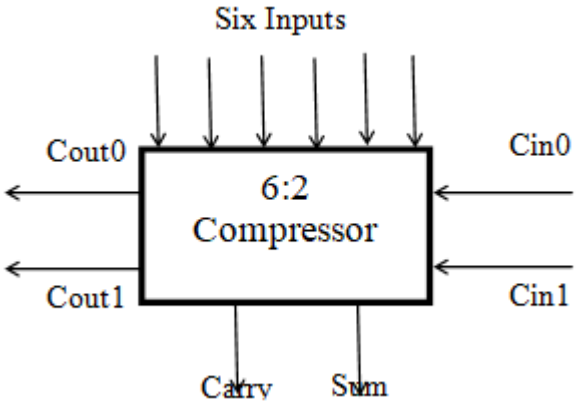

Figure 5: 6:2 Compressor

It consists of eight inputs out of which six are direct inputs and two are carry in bits from previous stage. Similarly, there are four outputs of which two are carry-out to the next stage and the other two are sum and carry bits. 6:2 compressors has been designed by cascading five 3:2 compressors.

4. Implementation of Full Adder Cell

Wallace tree multiplier circuit implementation is done in 45nm technology in Cadence Virtuoso tool. In the

multiplication process, partial products are generated by AND gates and partial product reduction is done with the help of compressors. Compressors are made up of full adders. Different logic styles have been chosen for implementing full adders. In this work full adders are implemented using 6 transistors logic. Wallace tree multiplier based on 6 T full adder has been tested for power consumption, delay, area utilisation and transistor count.

4.1 Results and Discussion

Table 1: Compression between Existing and Proposed Wallace Tree Multiplier

Parameters	Existing Wallace 8 bit multiplier (8T)	Proposed Wallace 8 bit Multiplier (6T)
Area (nm)	669	401
Power (nW)	52009	49632
Delay (ps)	6804	3783
No of Transistors	630	378

*8T – 8 Transistors, 6T – 6 Transistors

From the above table 1, it is clearly evident that, the area, power, delay and the number of transistors have been reduced for the proposed design of multiplier.

4.2 Conclusions

The reduction in complexity of Wallace tree multiplier has been done by utilising the compressor technique and by using less number of half adders. Comparison of proposed 6Transistor (6T) multiplier with the existing 8Transistor (8T) multiplier gives the result achievement of 40% reduction in the total area utilised, 5% reduction in the power consumption, 45% reduction in the delay and 40% reduction in the number of transistor utilised. This low power and high speed Wallace multiplier can also be used for and processor design.

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Author Profile

R Arthi received the B.E and M.E degrees in Electronics and Communication Engineering from Anna University Chennai in 2013 and 2015, respectively. She is working in KIT-Kalaingarkarunanidhi Institute of Technology as Assistant Professor. Her research Interest includes Low Power VLSI Design and Communication Engineering.

Dr. B. Senthilkumar received the B.E and M.E degrees in Electronics and Communication Engineering from Bharathiar University and Anna University Chennai in 2001 and 2006, respectively. During 2001-2015, he has been employed in Tamilnadu College of Engineering as Professor. Now he is working in KIT-Kalaingarkarunanidhi Institute of Technology as a Professor. His research Interest includes Circuit Optimization, and Communication Engineering.

R Gowrishankar received the B.E and M.TECH degrees in Electronics and Communication Engineering from Bharathiar University and SASTRA University in 2001 and 2004, respectively. During 2004-2008, he has been employed in Tamilnadu College of Engineering as Assistant Professor. Now he is working in KIT-Kalaingarkarunanidhi Institute of Technology as a Professor. His research Interest includes VLSI Design, Networking and Communication Engineering.

S. Tamilselvan received the B.E and M.E degrees in Electronics and Communication Engineering from Anna University Chennai in 2008 and 2013 respectively. During 2008-2012, he has been employed in Tamilnadu College of Engineering as Assistant Professor. Now he is working in KIT-Kalaingarkarunanidhi Institute of Technology as Associate Professor. His research Interest includes VLSI Design and Networking.

Dr. N. Sathish Kumar is a Professor in Electronics and Communication engineering Department is an accommodating and versatile individual with over 15 years of teaching in both UG and PG courses and 09 years of research experience with a solid commitment to the social and academic growth and development. He received his Ph.D degree from ANNA University, Chennai in the Field of MIMO Receivers-Wireless Communication, in year 2012. He completed his Master degree (Applied Electronics) programme from Government College of Technology, Coimbatore. He has published 08 papers in National conference and 3 in the international conference and 18 papers in reputed national and international journals. He has won Three ‘Best Paper’ awards for his research. He is a life member in various professional societies like IEEE (USA), IETE, ISTE, SSI.