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Design of Grid-Tied PV System with Single-Phase Transformerless Inverter Using Fuzzy Control Based Charge Pump Circuit Concept

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Abstract: ***In this paper proposes a single phase transformer less photovoltaic inverter for grid connect PV system. In this topology we are developing the concept of a charge pump circuit in order to eliminate the leakage current. We are utilizing the fuzzy controller in this paper. We are comparing the fuzzy controller with other controller. The neutral of the grid is directly connected to the negative polarity of the PV panel that creates a constant common mode voltage and zero leakage current. During the negative cycle, the charge pump circuit generates the negative output voltage of the proposed inverter. Therefore according to the proportional resonant control strategy is used to control the injected current. There are various advantage of the proposed inverter they are the neutral of the grid is directly connected to the negative terminal of the PV panel, so the leakage current is eliminated, its compact size; low cost; the used dc voltage of the proposed inverter is the same as the full-bridge inverter (unlike neutral point clamped (NPC), active NPC, and half-bridge inverters); flexible grounding configuration; capability of reactive power flow; and high efficiency. By using simulation result we can verify the concept of the proposed inverter and its practical application in grid-tied PV systems.***

Keywords: Charge pump circuit, grid-tied inverter, leakage current elimination, transformer less inverter, fuzzy control

1. Introduction

From the recent year we are developing the photovoltaic (PV) power systems have become very popular among the renewable energy sources, because they generate electricity with no moving parts, operate quietly with no emissions, and require little maintenance [1], [2]. Distributed grid-connected PVs are playing an increasingly role as an integral part of the electrical grid.

One of the important issues in the transformerless gridconnected PV applications is the galvanic connection of the grid and PV system, which leads to leakage current problems. Fig. 1 illustrates a single-phase grid-tied transformerless inverter with CM current path, where P and N are the positive and negative terminals of the PV, respectively.

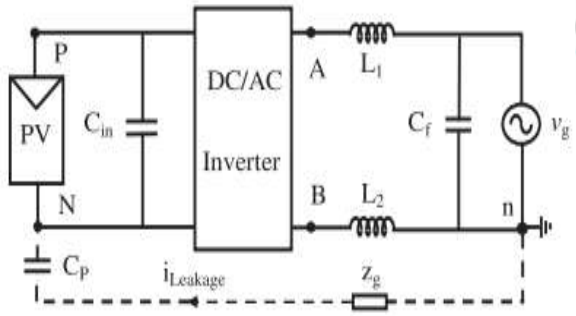


Figure 1: Block diagram of a single-phase grid-connected transformer less inverter with a leakage current path.

The vcm with two filter inductors (L1, L2) is calculated as follows:

$$v_{cm} = \frac{v_{An}+v_{Bn}}{2} + \frac{(v_{An}-v_{Bn})(L_1-L_2)}{2(L_1+L_2)} \quad (1)$$

Where vAn and vBn are the voltage differences between the midpoints A and B of the inverter to the dc bus minus terminal N, respectively. If L1 = L2 (asymmetrical inductor), vcm is calculated according to (1) and the leakage current appears due to a varying CMV. If L1 = L2 (symmetrical inductor), vcm is simplified to

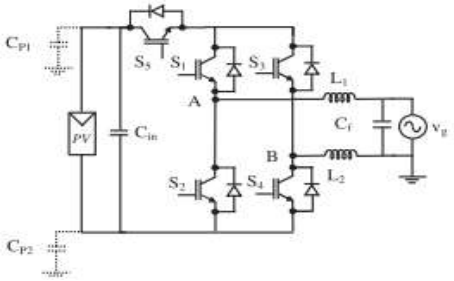
$$v_{cm} = \frac{v_{An}+v_{Bn}}{2} = Cons \quad (2)$$

In this state, the CMV is constant and the leakage current is eliminated. In some structures such as the virtual dc-bus inverter [10] and NPC inverter, one of the filter inductors is zero and only one filter inductor is used. In this state, after simplification of vcm, it will have a constant value according to (3) and the leakage current will be eliminated

$$v_{cm} = \frac{v_{An}+v_{Bn}}{2} + \frac{v_{An}-v_{Bn}}{2} = Const.(L_1 = 0) v_{cm} = \frac{v_{An}+v_{Bn}}{2} - \frac{v_{An}-v_{Bn}}{2} = Const.(L_1 = 0) \quad (3)$$

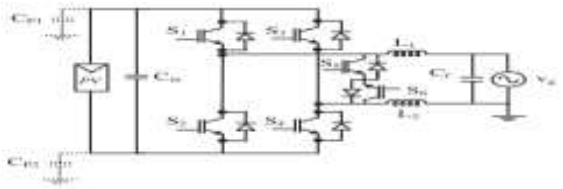
As shown in Fig. 2, there are various transformerless grid connected inverters based on the FB inverter in the literature to overcome these problems.

The H5 inverter that is a FB-based inverter topology, com pared to the conventional FB inverter, needs one additionalswitch (S5) on the dc side to decouple the dc side from the grid as shown in Fig. 2(a).



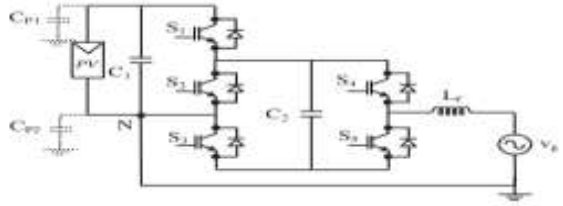
(a)

As shown in Fig. 2(b), the HERIC topology needs two extra switches on the ac side to decouple the ac side from the PV module in the zero stage.



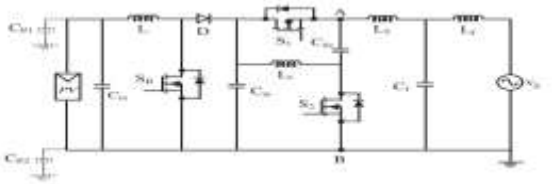
(b)

As shown in Fig. 2(c), the virtual dc-bus inverter is composed of five insulated-gate bipolar transistors (IGBTs), two capacitors, and one filter inductor Lf .



(c)

The virtual dc-bus generates the negative output voltage. The main drawback of this topology is that there is no path to charge the capacitor C2 during the negative cycle and this will cause a high output total harmonic distortion (THD). The topology presented, which is shown in Fig. 2(d), has a common ground with the grid.



(d)

Figure 2: Single-phase grid-tied transformerless PV inverter topologies: (a) H5 inverter, (b) HERIC inverter, (c) virtual dc-bus inverter [10], and (d) CM inverter proposed

However, the output voltage of this inverter is only two levels including positive and negative voltages without creating the zero voltage, which requires a large output inductor L2 and a filter. This paper introduces a new transformerless inverter based on charge pump circuit concept, which eliminates the leakage current of the grid-connected PV systems using a unipolar sinusoidal pulse width modulation (SPWM) technique.

2. Proposed Topology and Modulation Strategy

A. Charge Pump Circuit Concept

The concept of a simple charge pump circuit to be used in the proposed topology to generate the inverter negative output voltage is shown in Fig. 3. The circuit consists of two diodes (D1, D2) and two capacitors (C1, C2). The capacitor C1 is used to couple the voltage point of A to the node D.

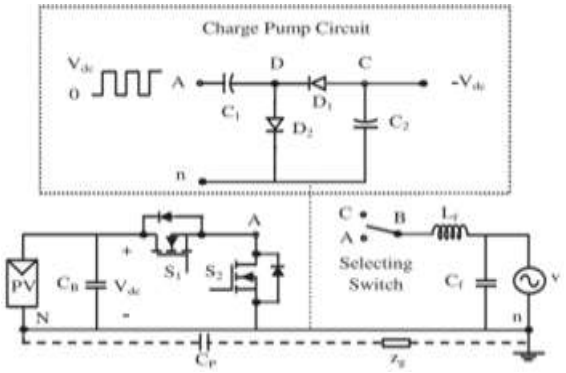


Figure 3: Schematic diagram of the proposed inverter including the charge pump circuit.

In steady state, the output voltage of the negative charge pump circuit (vCn) can be derived by

$$v_{Cn} = -V_{dc} + V_{cut-in-D1} + V_{cut-in-D2} \quad (4)$$

Where Vdc is the input voltage, Vcut−in−D 1 and Vcut−in−D 2 are the cut-in voltages of the diodes D1 and D2, respectively. For high power applications, these values can be negligible.

The charge pump circuit in the transformerless inverter has the following characteristics for grid-tied applications.
1) This circuit has a common line with the negative terminal of the input dc voltage and the neutral point of the grid that causes the leakage current to be eliminated.
2) The charge pump circuit has no active device and it has a lower cost for grid-tied applications.

B. Proposed Topology

As shown in Fig. 4, the proposed topology consists of four power switches (S1 − S4), two diodes (D1, D2), two capacitors (C1, C2) based on the charge pump circuit.

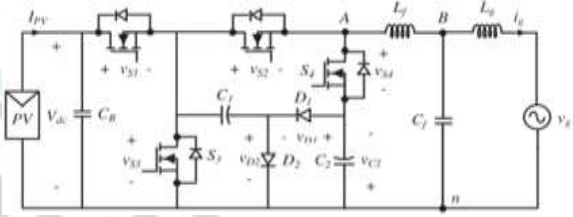


Figure 4: Proposed single-phase transformerless grid-connected inverter

This new topology is modulated using simple SPWM. Fig. 5 shows the gate drive signals for the proposed inverter under the current lagging condition. According to the direction of the inverter output voltage and output current, theoperation of the proposed inverter is divided in four regions as shown in Fig. 6.

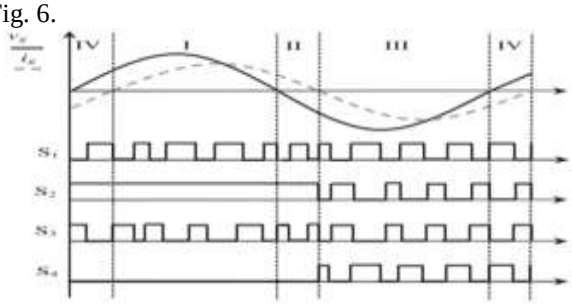
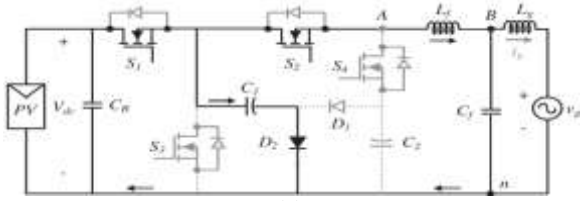
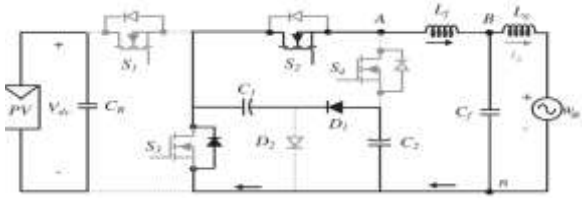


Figure 5: Switching pattern of the proposed topology with reactive power flow.

Region I: the inverter output voltage and the output cur rent are positive; energy is transferred from dc side to grid side as shown in Fig. 6(a).

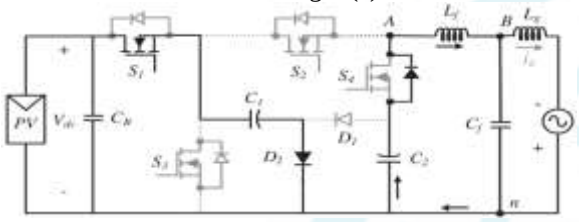


(a)

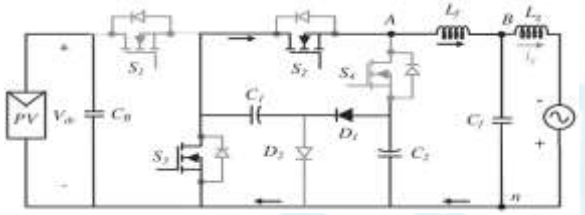


(b)

Region II: the inverter output voltage is negative and the output current is positive; energy is transferred from grid side to dc link as shown in Fig. 6(c).



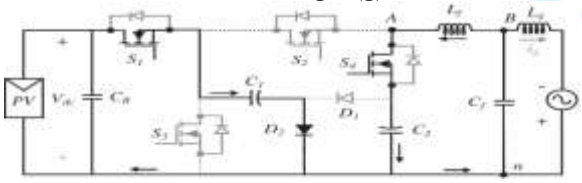
(c)



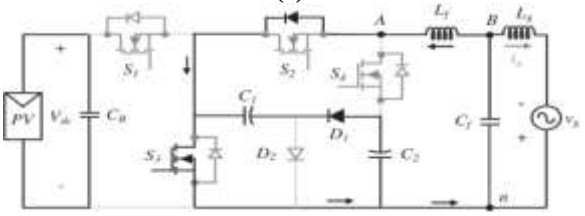
(d)

Region III: the inverter output voltage and the output current are negative; energy is transferred from dc link to grid side as shown in Fig. 6(e).

Region IV: the inverter output voltage is positive and the output current is negative; energy is transferred from grid side to dc side as shown in Fig. 6(g)

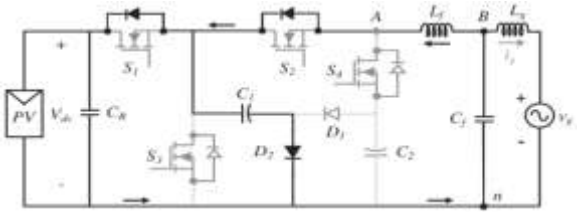


(e)

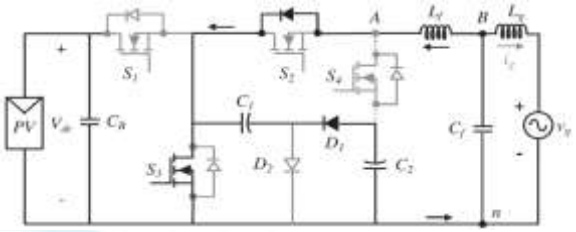


(f)

When the switches S1 and S2 are ON, the output voltage of the inverter (vAn) will be + Vdc (positive state) as shown in Fig. 6(a) and (g). During this time interval, diode D1 is reverse biased and D2 is ON, so the capacitor C1 is charged through diode D2 and the voltage across the capacitor C2 maintains to be constant. In this state, when the switches S2 and S3 are ON, vAn will be 0 (zero state) as shown in Fig. 6(b) and (h).



(g)



(h)

Figure 6: Operational stages of the proposed inverter during (a),(b) region I,(c),(d) region II,(e),(f) Region III and (g),(h) region IV $(a)v_{An} = +V_{dc}, i_g > 0$. $(b)v_{An} = 0, i_g > 0. (c)v_{An} = -V_{dc}, i_g > 0. (d)v_{An} = 0, i_g > 0. (e)v_{An} = -V_{dc}, i_g < 0. (f)v_{An} = 0, i_g < 0. (g)v_{An} = +V_{dc}, i_g < 0. (h)v_{An} = 0, i_g < 0$

In the regions II and III, the negative and zero voltage levels are produced. Fig. 6(c) and (e) shows the equivalent circuit that S4 and S1 are ON.

The voltage across the capacitor C1 can be kept constant in this state by the modulation strategy. In this period, the circuit operation of the zero state is similar to the zero state of positive half-period of the grid as shown in Fig. 6(b) and (h). In this case, the charging time constant of capacitor C2 (τC 2) can be expressed as follows:

$$\tau_{C2} = R_{e1} C_{e1} \quad (5)$$

The current through capacitors (iCapacitors) is calculated by

$$i_{Capacitors} = C_{e1} \frac{V_{C1} - V_{C2}}{\tau_{C2}} \quad (6)$$

According to (5), the charging time constant of C2 is larger than its natural discharging time constant and VC 1 − VC 2 has a very small value in steady state.

3. Analysis of the Proposed Topology

A. Current Stress Analysis and Capacitors Design

A current stress analysis of the proposed topology is presented in this section. The maximum value of the current stress occuron the switches S1 and S3, because the capacitor C1 is charged through switch S1 and the capacitor C2 is charged through switch S3. Therefore the simulation results of the current in the switches S1 and S3 for an output power of 500 W are shown in Fig. 7.

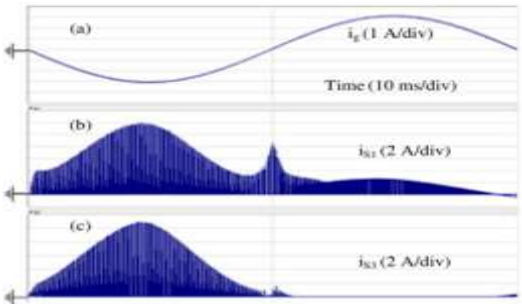
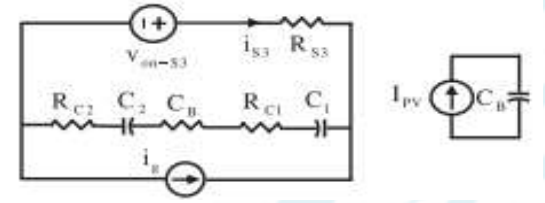


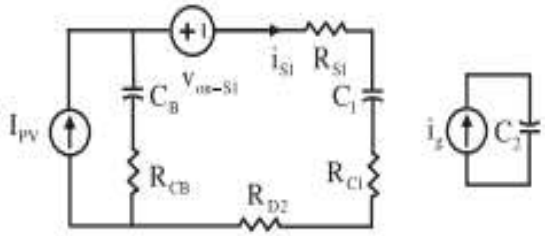
Figure 7: Simulations of the current of switches: (a) grid current (ig) [1 A/div], (b) (iS 1) [2 A/div], and (c) (iS 3) [2 A/div].

The maximum value of the current in these switches occurs at the negative state in simulation results as shown in Fig. 7.

According to the electric circuit theory, the grid voltage in series with a grid-side inductor (Lg) can be equivalent with the current source (ig) as shown in Fig. 8.



(a)



(b)

Figure 8: Equivalent circuit of the proposed converter during (a) zero state and (b) negative state.

According to Fig. 8(a), at the zero state

$$\frac{dv_{diff,1}}{dt} = \frac{v_{diff,1} - R_{s3} i_g}{(R_{e1} + R_{s3}) C_{e1}} \quad (7)$$

$$\frac{dv_{diff,2}}{dt} = \frac{I_{PV}}{C_B} - \frac{v_{diff,1} - R_{s3} i_g}{(R_{e1} + R_{s3}) C_1} \quad (8)$$

According to Fig. 8(b), in the negative state

$$\frac{dv_{diff,1}}{dt} = \frac{R_{Cb} I_{PV} + v_{diff,2}}{(R_{cb} + R_{e2}) C_1} + \frac{i_g}{C_2} \quad (9)$$

$$\frac{dv_{diff,2}}{dt} = \frac{I_{PV}}{C_B} + \frac{R_{Cb} I_{PV} - v_{diff,2}}{R_{e2} C_{e2}} \quad (10)$$

where in (8)–(11), Re2 and Ce2 will be as follows:

$$R_{e2} = R_{D2+} R_{S1} + R_{C1} + R_{CB}, C_{e2} = \frac{C_1 C_B}{C_1 + C_B} \quad (11)$$

By using the averaging method at the switching cycle Ts, and linearizing (8)–(11), the average value of iS 1 and iS 3 at the negative and zero states is equal to (13) and (14), respectively:

$$\frac{dv_{diff,1}}{dt} = \left(1 + s(t)\right) \frac{v_{diff,1} - R_{s3} i_g}{(R_{e1} + R_{e2}) C_{e1}} - s(t) \left(\frac{R_{CB} I_{PV} + v_{diff,2}}{(R_{cB} + R_{e2}) C_1} + igC2 \right.$$

$$\frac{dv_{diff,2}}{dt} = \left(1 + s(t)\right) \left(\frac{I_{PV}}{C_B} - \frac{v_{diff,1} - R_{s3} i_g}{(R_{e1} + R_{e2}) C_1} \right) - s(t) \left(\frac{I_{PV}}{C_B} + RCBIPV + vdiff,2Re2 + Ce2 \right. \quad (12)$$

where s(t) denotes the switching state function given as follows:

$$s(t) = \begin{cases} 1, & when the circuit is at positive state \\ 0, & when the circuit is at zero state \\ -1, & when the circuit is at negative state \end{cases}$$

The average current of iS 1 and iS 3 during Ts can be found as follows:

$$\langle i_{s1} \rangle_{T2} = \frac{v_{diff,1} T_s + R_{s3} \langle i_g \rangle T_s}{R_{e1} + R_{s3}} \quad (13)$$

$$\langle i_{s1} \rangle_{T2} = \frac{v_{diff,2} T_s + R_{cB} I_{PV}}{R_{e2}} \quad (14)$$

The simulation results of the current flowing through the switches S1 and S3 for the output power 500 W are shown in Fig. 7. The value of the current that passes through S1 and S3 to reach to its maximum at the negative state is shown in this figure too. At the negative state,

$$\langle i_{s1,max} \rangle_T = \frac{1}{2} \left(\frac{C_1}{C_1 + C_2} + 1 \right) \left(\frac{M I_m}{1 - M} + \frac{T_s}{R_{e1} C_{e1}} \frac{1 - M}{2} \right) \quad (15)$$

$$\langle i_{s3,max} \rangle_T = \frac{1}{2} \left(\frac{C_1}{C_1 + C_B} + 1 \right) \left(\frac{M I_m}{1 - M} + \frac{T_s}{R_{e2} C_{e2}} \frac{1 - M}{2} \right) \quad (16)$$

Equations (22) and (23) indicate that the values of C1/(C1 + C2) and C1/(C1 + CB) should be calculated small enough, and the values of the Re1Ce1 and Re2Ce2 should be smaller than the switching period in order to minimize the current stress on the switches.

These values can be limited by a small resistor or a small inductor between the capacitors if needed. The relationship between the voltage and current passing through the capacitors is calculated by

$$i_C = C \frac{\Delta v_c}{\Delta t} \quad (17)$$

The required capacitance of C1 and CB for the proposed in verter can be derived by equaling the capacitor power magnitude to the grid power ripple magnitude. The capacitance C1 and CB can be calculated as follows:

$$C_1 or B = \frac{I_{C1} or B\,(\max)}{\wedge (V_r V_n) f} \quad (18)$$

where IC 1max and IC B max are the maximum current that passes through the capacitors C1 and CB , respectively.

B. Conduction and Switching Losses of Power Devices

During the positive power cycle, the grid current flows through switches S1 and S2 and the capacitor C1 is charged through diode D2 at the positive state as shown in Fig. 6(a) and (g). The capacitor C1 is charged through diode D2 and switch S1 at the negative state as shown in Fig. 6(c) and (e). The voltage drop of the power devices can be derived by

$$MOSFET: v_{DS}(t) = i(t) R_{DS} \quad (19)$$

$$Diode: \; v_{AK}(t) = V_F + i(t) R_{AK} \quad (20)$$

where vDS is the drain source voltage drop of the MOSFET, RDS is the drain source resistance of the MOSFET during on the state operation, vAK is the anode cathode voltage drop of the diode, VF is the equivalent voltage drop under zero current condition of the diode, RAK is the anode cathode resistance of the diode during the on state, and i(t) is the grid current. The average value of the conduction losses of the MOS FET switch (PMOSFET Cond) during half of the fundamental period is calculated by

Table 1: Duty Ratio of Each Conducting Device

Semiconductor devices	$duty\ ratio\ (d)$ $positive\ cycle\ (v_g > 0)$	$negative\ cycle\ (v_g 0)$
S_1	$M \sin \omega t$	$M \sin \omega t$
S_2	1	$1 - M \sin \omega t$
S_3	$M \sin \omega t$	$1 - M \sin \omega t$
S_4	0	$M \sin \omega t$
D_1	0	$M \sin \omega t$
D_2	$M \sin \omega t$	0

$$P_{MOSFET\_Cond} = \frac{1}{\pi}\int_0^{\pi} v_{DS}(t) i(t) d_{MOSFET}(t)\, d\omega t \quad (21)$$

The average value of the conduction loss in the diode (PDiodeCond) during the on state mode is calculated by

$$P_{Diod\,e_{Cond}} = \frac{1}{\pi}\int_0^{\pi} v_{AK} i(t) d_{Diodes}(t) d\omega t$$

$$= \frac{1}{\pi}\int_0^{\pi} v_F i(t) R_{AK} i(t) d_{Diodes}(t) d\omega t \quad (22)$$

The device manufacturer and circuit parameters for efficiency evaluation of proposed inverter are listed in Table II.

Table 2: Specifications and Power Devices For Efficiency Evaluation

Parameter	Value
Input Voltage	400 V
Grid voltage/frequency	220V/50 HZ
Rated power	500 W
Ac Output Current	2.3A
Switching frequency	24 KHZ
Duty ratio (M)	0.78

The switching losses of the MOSFET switch can be found as follows:

$$P_{MOSFET\_SW} = f_{SW} E_{OSS} V_F \quad (23)$$

Where Eoss is the stored energy that can be achieved from the datasheet that is equal to 45 μJ. The total switching losses of the switches in the proposed inverter can be derived as follows:

$$P_{Total\ -SW} = 4 f_{SW} E_{OSS} V_F = 3.46\ W \quad (24)$$

C. Conduction Losses in the Capacitors

The ESR of the capacitors of the proposed inverter is achieved from aluminum electrolyte capacitor datasheets and it is divided into two parts. The second part of the conduction losses is related to the inrush current during the charging of the capacitors. These losses can be defined as follows:

$$P_{CAP\_Cond\_1} = \frac{2(R_{C1}+R_{CB})}{\pi}\int_0^{\pi} d_c(t) i_{s1}^2(t) d\omega t \quad (25)$$

$$P_{CAP\_Cond\_2} = \frac{2(R_{C1}+R_{C2})}{\pi}\int_0^{\pi} d_c(t) i_{s3}^2(t) d\omega t \quad (26)$$

where dc(t) is the duty ratio of the capacitor.

D. Control Scheme

The control strategy of the proposed grid-tied single-phase inverter is shown in Fig. 9. It contains two cascaded loops ; the first loop is an inner control loop, which has the responsibilities to generate a sinusoidal current and the outer control loop is implemented for the current reference generation, where the power is controlled. The transfer function of this controller can be found as follows:

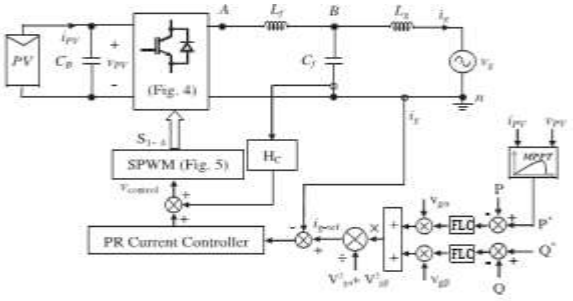


Figure 9: Control block diagram of the proposed single-phase grid-tie inverter based on single-phase PQ theory.

$$G_{PR(s)} = K_p + \frac{2K_r}{s^2+\omega^2} \quad (27)$$

where k p is the proportional gain, kr is the fundamental resonant gain, and ω is the resonant frequency. According to the single-phase PQ theory the current reference can be produced by regulating the active and reactive powers. The active power (P) and reactive power (Q) for the proposed topology can be calculated by

$$P = \frac{v_{g\alpha} i_{g\alpha} + v_{g\beta} i_{g\beta}}{2},\ Q = \frac{v_{g\alpha} i_{g\alpha} - v_{g\beta} i_{g\beta}}{2} \quad (28)$$

where v gα, vgβ , igα, and igβ are the α and β components of grid voltage and current, respectively. The active power and reactive power references (P∗ and Q∗) can be tuned by the operators {R– 3} or in the control unit, when the MPPT control is activated. If PI controllers are used for power regulations, the grid current reference (ig-ref) can be derived as follows [24]:

$$i_{g-ref} = \frac{1}{v_{g\alpha}^2 + v_{g\beta}^2}\begin{bmatrix} v_{g\alpha} & v_{g\beta} \end{bmatrix}\begin{pmatrix} G_p(s) & (P-P^*) \\ G_q(s) & (Q-Q^*) \end{pmatrix} \quad (29)$$

where G p(s) and Gq(s) are the PI controllers for active power and reactive power, respectively.

The LCL filter is adopted as the grid interfaced filter in this proposed topology. High output current quality in the proposed inverter can be obtained if the output filter is configured correctly. The inverter-side inductor (Lf) value is calculated by considering 10–20% of the ripple on the output current, which is given by

$$L_f = \frac{(v_{dc} - v_{An})(M \sin\ \omega t)}{f_{SW}\,\Delta i_L} \quad (30)$$

Where fsw is the switching frequency and ΔiL represents the peak-to-peak ripple current on the Lf . The inverter output volt age (vAn) can be calculated as follows:

$$v_{An} = M V_{dc} \sin \omega t \quad (31)$$

By replacing (39) with (38) and simplifying it, we have

$$L_f = \frac{(v_{dc})(RF)}{f_{sw}\,\Delta i_L} \quad (32)$$

where RF is the ripple current and can be calculated from

$$RF = M \sin \omega t - M^2 sin^2 \omega t \quad (33)$$

The maximum achievable value of modulation index (M) is RFmax = 0.25 [26]. The maximum value of the filter capacitor is calculated by (42), limiting to be less than 5% of the nominal value [27]

$$C_{F,max} = \frac{0.05 P_n}{2\pi f V_{rms}^2} \quad (34)$$

Where Pn is the nominal power, Vrms denotes the root mean square (RMS) grid voltage, and f presents the grid frequency. There is a relation between the inverter-side

inductor (Lf) and the grid side (Lg). This value is determined with the ratio be tween the ripple attenuation (r) as described in [28]

$$L_g = rL_f \quad (35)$$

The grid-side inductor (Lg) value can be determined by

$$10f \leq f_{res} \leq 0.5f_{sw} \quad (36)$$

The resonant frequency for the LCL filter is given by

$$f_{res} = (1/2\pi)\sqrt{(L_f + L_g)/L_f L_g C_f} \quad (37)$$

The active damping is used to smooth the resonance peak of the LCL filter as shown in Fig. 9. A block diagram of the control system is shown in Fig. 10. The Bode diagram of the transfer function from vcref to ig is defined by G(s). This diagram is shown in Fig. 11 in order to demonstrate the effect of active damping by the filter capacitor current (Hcic)

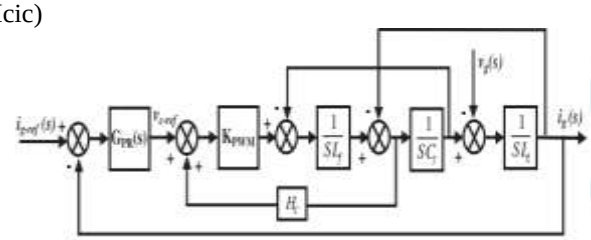


Figure 10: Control diagram of the injected current with capacitor current feedback active damping.

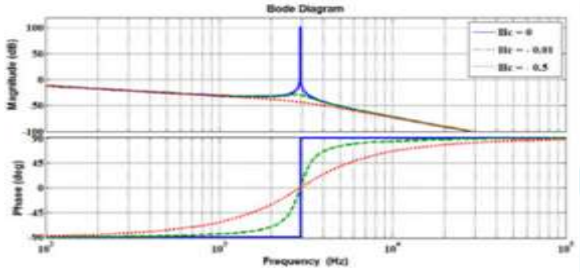


Figure 11: Bode plot of the system in the case of different values for the active damping gain HC

$$G(s) = \frac{K_{PWM}\, G_1(s)}{1 + H_C K_{PWM}\, C_f L_g G_1(s) S^2} \quad (38)$$

and K pwm = 1 and HC is the active damping gain.

E. Comparison with Other Known Topologies

A comparison of the transformerless inverter structures with respect to number of semiconductor devices, passive elements, THD of the current, and number of switches in the current

4. Fuzzy Logic Controller

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

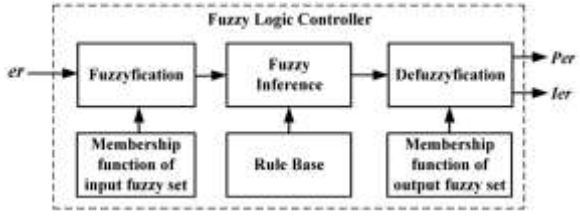


Figure 13:.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

Table 3: Fuzzy Rules

e / Δe	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (39)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (40)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u = -[\alpha E + (1-\alpha)*C] \quad (41)$$

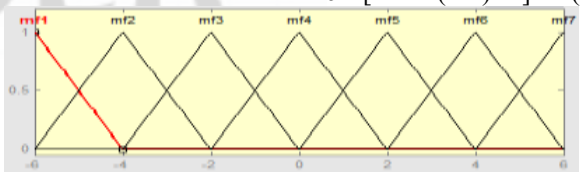


Figure 14: Input error as membership functions

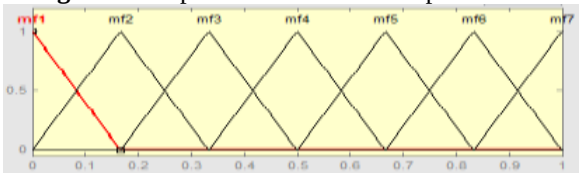


Figure 15: Change as error membership functions

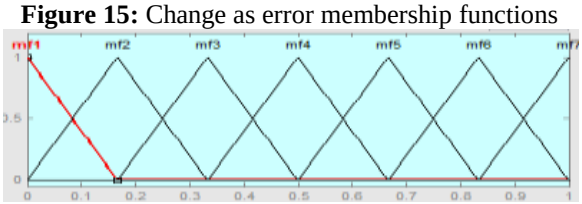


Figure 16: Output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

5. Simulation Results

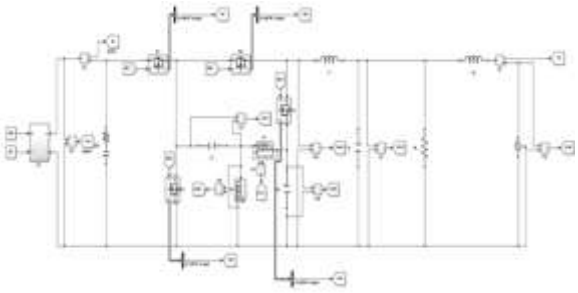


Figure 17: Simulation block diagram of proposed single-phase transformerless grid-connected inverter

In fig 17 the proposed grid connected inverter will operate with the unity power factor(PF = 1) will seen in simulation results. The simulation results of the proposed grid-connected inverter with unity power factor (PF = 1) operation are presented in Fig18

Table 4: Parameters For The 500 W

Parameter	Value	Parameter	Value
Power rating (P)	500 W	Capacitance (C_1)	220 μF, 500 V
Input voltage (V_{dc})	400V	Capacitance (C_2)	330 μF, 500 V
Output voltage (v_{Bn})	220 V (RMS)	L filter (L_f)	4 mH
Input capacitor (C_B)	470 μF, 500 V	C filter (C_f)	2.2 μF
Power switches ($S_1 - S_4$)	C2M0080120D, SiC MOSFET	L_g	2 mH
Diodes (D_1, D_2)	C3D10060A Schottky Diode	Switching frequency (f_s)	24 kHz

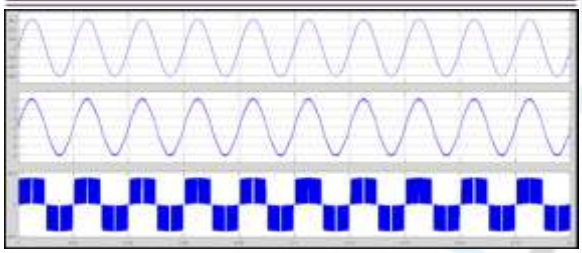


Figure 18: Simulation results of the proposed topology with unity power factor (PF = 1) operation. (a) vg [500 V/div], (b) ig [5 A/div], (c) vA n [500 V/div], and (d) fast Fourier transform analysis of ig [50 V/div and 125 Hz/div].

From Fig. 18, it is clear that the output current and voltage of the proposed inverter are highly sinusoidal with low harmonic distortion due to the three-level inherency of the output voltage. The current harmonic distribution is demonstrated in Fig. 13. Figs. 19 and 20 demonstrate the simulation results for the inverter operating under current lagging condition (PF = + 0.8) and leading condition (PF = – 0.8), respectively.

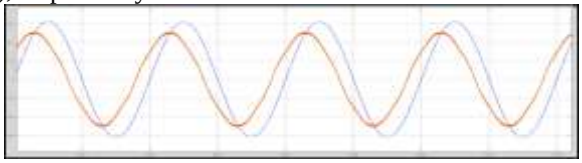


Figure 19: Simulation results of the proposed topology with lagging power factor operation. (a) vg [500 V/div] and (b) ig [2 A/div].

Figure 20: Simulation results of the proposed topology with leading power factor operation. (a) vg [500 V/div] and (b) ig [2 A/div]

The partial enlargement of the grid current ig, grid voltage vg, and three level output voltage vAn is provided in Fig. 21. It is clear that the pulse duration of the output voltage (vAn) is in agreement with the switching frequency. The voltage stress of the capacitors and diodes is shown in Fig. 22.

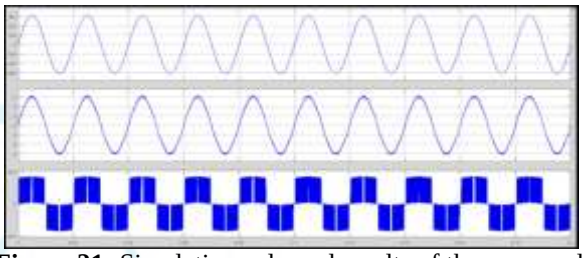


Figure 21: Simulation enlarged results of the proposed topology. (a) vAn [500 V/div], (b) vg [250 V/div], and (c) ig [5 A/div], time [400 μs/div]

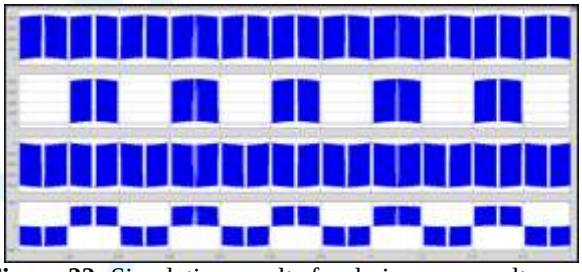


Figure 22: Simulation results for drain source voltage of switches. (a) vS 1 [250 V/div], (b) vS 2 [500 V/div], (c) vS 3 [250 V/div], and (d) vS 4 [500 V/div].

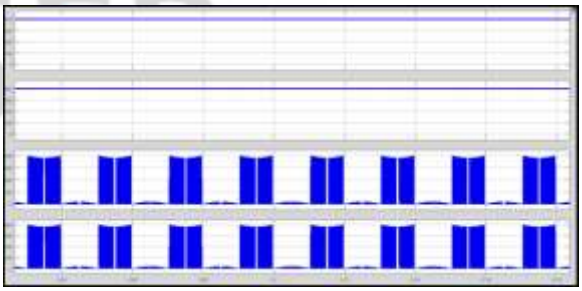


Figure 23: Simulation results of the capacitor and diode voltages. (a) vC 1 [250 V/div], (b) vC 2 [500 V/div], (c) vD 1 [250 V/div], and (d) vD 2 [250 V/div]

Fig. 23 (a)–(c) shows the simulation waveforms of the grid voltage vg, the grid current ig, and the CM voltage vCM in the proposed topology.

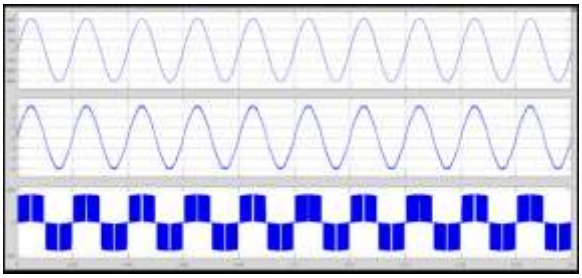


Figure 24: Simulation results of the proposed topology. (a) vg [250 V/div], (b) ig [5 A/div], and (c) CMV [200 V/div].

The performance of the control strategy is confirmed by ap plying a step change to the proposed inverter. A PR current controller is adopted with ki = 2000 and kp = 20 as shown in (35). Fig. 25 shows the performance of the proposed inverter under the load step change. From fig: 26 total harmonics distortion of the proposed topology.

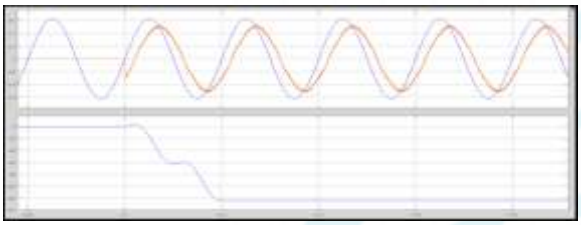


Figure 25: Simulation results of the proposed topology in dynamic state. (a) vg [250 V/div], (b) ig [10 A/div], and (c) active power (P) [400 W/div].

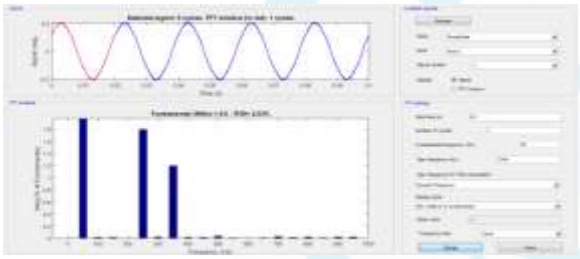


Figure 26: Total harmonics distortion

6. Conclusion

In this paper we are implementing a new single-phase transformer less inverter for a grid-tied PV system using a charge pump circuit concept with the fuzzy controller. Therefore the main concept of the proposed system is to generate the negative output voltages which have been developed in this proposed inverter. Here we are using the fuzzy logic controller for the better performance because the fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. Therefore we are developing the proposed topology which is similar to the neutral line in the grid; therefore the leakage current will be suppressed and the transformer is eliminated. Moreover the proposed topologies have the capability to deliver the required reactive power into the grid. Therefore the proposed topology is used to realize the mini mum number of components and higher power density can be achieved with lower design cost. By using the simulation result we can verify the proposed system.

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