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Design and Performance Analysis of CNTFET Based Asymmetric Threshold *Stacked* Leakage Reduction Technique for NVSRAM Cells

Uma Maheshwar Janniekode[1], Rajendra Prasad Somineni[2]

[1]Research Scholar, Department of ECE, VNR Vignana Jyothi Institute of Engineering and Technology, JNTU Hyderabad, Telangana, India
Email: *j.umamahesh21[at]gmail.com*

[2]Professor, Department of ECE, VNR Vignana Jyothi Institute of Engineering and Technology, JNTU Hyderabad, Telangana, India
Email: *rajendraprasad_s[at]vnrvjiet.in*

Abstract: ***The Asymmetric Threshold and Stacking (AT-S) technique has already proved effective for leakage mitigation in CMOS memories. In this work we extend and quantify its impact on Carbon Nanotube Field-Effect Transistor (CNTFET) implementations of Non-Volatile SRAM (NVSRAM), including a recently reported 8T3R NVSRAM cell. Standard 6T/8T NVSRAMs and the 8T3R architecture were modelled in a 16 nm CNTFET process and benchmarked, under identical bias and workload conditions, against functionally equivalent 16 nm CMOS designs. All circuits were simulated with Synopsys HSPICE. Applying AT-S to CNTFET NVSRAMs yielded up to 69 % average leakage-power reduction and a 60 % drop for the high-performance 8T3R cell, while preserving read/write delay and static noise margin. Relative to their CMOS counterparts, CNTFET-based AT-S cells delivered an additional ≈10 % leakage saving and superior process-voltage-temperature robustness. These results demonstrate that (i) the AT-S technique remains highly effective when ported from CMOS to emerging CNTFET technology, and (ii) CNTFET devices further amplify the power-efficiency gains, making the combined solution a compelling candidate for next-generation low-power, high-speed non-volatile memories.***

Keywords: CMOS, SRAM, NVSRAM NVM, CNTFET, HSPICE, ReRAM

1. Introduction

Complementary Metal-Oxide Semiconductor (CMOS) technology has long been the foundation of digital electronics due to its scalability and cost-effectiveness. However, scaling CMOS below the 20 nm node introduces challenges like increased leakage power, short-channel effects, process variability, and performance degradation [1], [2]. To overcome these issues, Carbon Nanotube Field-Effect Transistors (CNTFETs) have emerged as a promising alternative. CNTFETs provide near-ballistic transport, high carrier mobility, low subthreshold swing, and superior electrostatic control, making them ideal for low-power, high-performance applications, particularly in nanoscale memory design [3], [4].

Conventional Static Random-Access Memory (SRAM) is fast and power-efficient but suffers from volatility and high leakage in standby mode, especially at smaller technology nodes [5]. These drawbacks have increased interest in Non-Volatile SRAM (NVSRAM), which combines a traditional SRAM core with non-volatile elements. NVSRAM offers instant-on capability, data retention during power-off, and improved power efficiency for energy-limited applications like IoT, biomedical devices, and edge computing [6].

Several non-volatile memory (NVM) technologies have been explored for NVSRAM integration, including Flash, FeRAM, MRAM, Phase-Change Memory (PCM), and Resistive RAM (ReRAM) [7]. ReRAM stands out due to its simple structure, CMOS compatibility, fast switching, low voltage operation, and excellent scalability [8], [9]. ReRAM-based NVSRAM uses materials like HfO_2 and TiO_2 for resistive switching, enabling data retention. While ReRAM-CMOS integration has been widely studied, combining ReRAM with CNTFETs offers even greater benefits. CNTFET-based NVSRAMs with ReRAM achieve reduced leakage, improved energy efficiency, and faster read/write speeds, all while supporting high integration density [10], [11].

This study adapts the Asymmetric Threshold and Stacking (AT-S) technique, originally used for leakage reduction in CMOS NVSRAM—for CNTFET-based NVSRAMs, including the 8T3R architecture. We evaluate ReRAM integration in both CMOS and CNTFET-based NVSRAM cells. Simulations at the 16 nm node using Synopsys HSPICE assess leakage power, performance, and stability. Results show that the CNTFET + ReRAM + AT-S combination delivers superior energy efficiency and performance, confirming its potential for future ultra-low-power memory applications

2. Emerging Technologies

a) Resistive Random Access Memory (ReRAM)

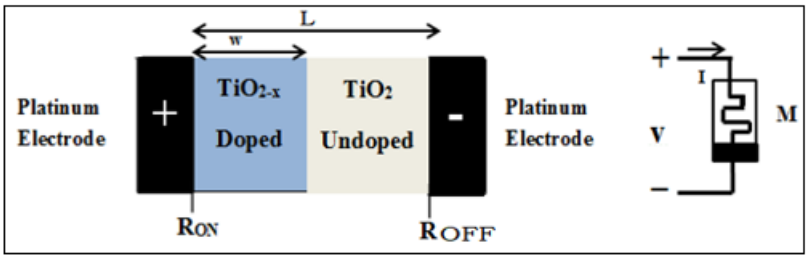
Resistive Random Access Memory (ReRAM) is a non-volatile memory technology that operates by changing the resistance of a metal-oxide layer. Its origin is rooted in the memristor concept introduced by Leon Chua in 1971, defined as a two-terminal device that maintains a functional relationship between electric charge qq and magnetic flux ϕ[12] as shown in Fig. 1.

The device stores information by altering its memristance M, which governs its current-voltage behavior as:

$$i(t) = X_m^{-1}.\ v(t)$$

where Xm is the internal state variable representing the memristance.

Figure 1 Memristor structure and its circuit symbol in which thick lines represent doped layer



A practical model views the memristor as two resistors in series: RON (low resistance) and ROFF (high resistance), with a boundary w determining the active region. The equivalent resistance is:

$$R(w) = R_{ON} \times \frac{w}{L} + R_{OFF}\left(1 - \frac{w}{L}\right) \quad (1)$$

The memristance as a function of charge q(t) is modelled as:

$$M(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON} q(t)}{L^2}\right) \quad (2)$$

where: μv: mobility of oxygen ions, L: total device length.

The I-V relationship becomes:

$$V(t) = \left(R_{ON} \times \frac{w(t)}{L} + R_{OFF}\left(1 - \frac{w(t)}{L}\right)\right) i(t) \quad (3)$$

with w(t) evolving as:

$$w(t) = \frac{\mu_V R_{ON}}{L} q(t) \quad (4)$$

This switching is based on the drift of oxygen vacancies forming or rupturing a conductive filament in the oxide layer (e.g., TiO_2), toggling between LRS and HRS [13][14].

b) Carbon Nanotube Field-Effect Transistor (CNTFET)

As silicon-based CMOS technology nears its physical and scaling limits, emerging nanotechnologies are being explored for future VLSI systems. Among them, Carbon Nanotube Field-Effect Transistors (CNTFETs) stand out due to their superior electrical, mechanical, and thermal properties. CNTFETs utilize semiconducting single-walled carbon nanotubes (SWCNTs) as channel material, replacing silicon. Their quasi-one-dimensional structure enables near-ballistic transport, high carrier mobility, and steep subthreshold slopes, resulting in high-speed, low-power, and high-density nano electronic circuits.

With configurable chirality vectors (n, m) that define their bandgap, CNTFETs offer better control over switching behaviour. They also exhibit reduced leakage current and are less affected by short-channel effects than traditional MOSFETs, making them ideal for nanoscale logic and memory applications [15][16]. Figure 2 depicts the structure of carbon nanotubes, which are cylindrical in shape and possess unique physical and electrical traits.

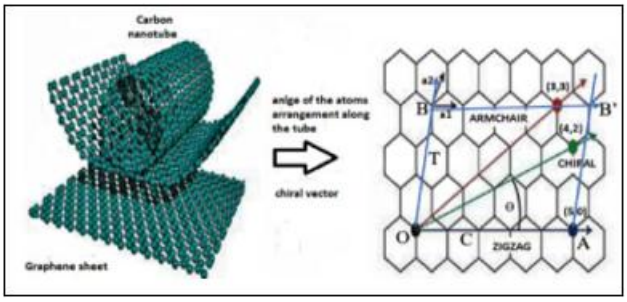


Figure 2: Rolling Graphene sheet to create Carbon Nanotube

c) Design Parameters of CNTFETs

To accurately model and design CNTFET-based circuits, several device-level parameters must be considered. These include chirality, diameter, channel length, threshold voltage, and capacitances. The Table 1 summarizes key parameters along with their governing equations. CNTFETs are often considered for integration with emerging memories like ReRAM to build energy-efficient non-volatile logic and storage subsystems [17][18].

Table 1: CNTFET Design Parameters and Equations

Parameter	Typical Value	Equation / Formula	Description
Chirality (n, m)	(19, 0)	—	Defines the CNT structure and its semiconducting or metallic nature.
CNT Diameter d	~1.5 nm	$d = a\frac{\sqrt{m^2+n^2+mn}}{\Pi} = \frac{Ch}{\Pi} = 0.246$	Affects threshold voltage and bandgap.
Bandgap Eg	~0.6 Ev	$E_g = \frac{2aV_\Pi}{d} = V_\Pi = 3ev$	Inversely proportional to diameter.
Threshold Voltage Vth	0.2–0.3 V	$Vth = \frac{E_g}{2q}$	Depends on the CNT bandgap.
Channel Length L	16 nm	—	Affects short-channel effects and delay.
Gate Oxide Thickness	1.5 nm	$C_{ox} = \frac{2\pi\varepsilon_{ox}L}{\ln(2h/r)}$	Affects gate control over the channel.
Quantum Capacitance CQ	—	$C_Q = \frac{4q^2}{hv_F}$	Arises from 1D density of states of CNT.
Total Gate Capacitance Cg	—	$C_g = (\frac{1}{C_{ox}} + \frac{1}{C_Q})$-1	Combination of oxide and quantum capacitance.

Mean Free Path λ	~200 nm		Distance carriers travel without scattering; enables ballistic transport.
ON Resistance RON	~6.5 kΩ	$RON=\frac{h}{4q^2}$	Minimum resistance in ballistic regime.
Drain Current IDS	—	$IDS=\frac{h}{4q^2}$ (VGS−Vth)	Describes current in ballistic transport mode.

3. Design of AT-S NVSRAM Cells Using CNTFET

As CMOS technology scales down to the nanometer regime, it faces several limitations such as increased leakage, short-channel effects, and reduced gate control. Carbon Nanotube Field Effect Transistor (CNTFET) technology has emerged as a promising alternative, offering superior electrical properties, ballistic transport, and scalability beyond silicon limits. This section presents the design of an Asymmetric Threshold Static Random Access Memory (AT-S SRAM) cell using CNTFETs, highlighting key design parameters and performance benefits.

a) CNTFET-Based AT-S SRAM Cell Design

The Figure 3. below illustrates the AT-S SRAM cell implemented using CNTFET devices. The circuit is similar to a conventional 6T SRAM structure but uses transistors with asymmetric threshold voltages and different chirality values, exploiting the threshold-voltage tunability of CNTFETs.

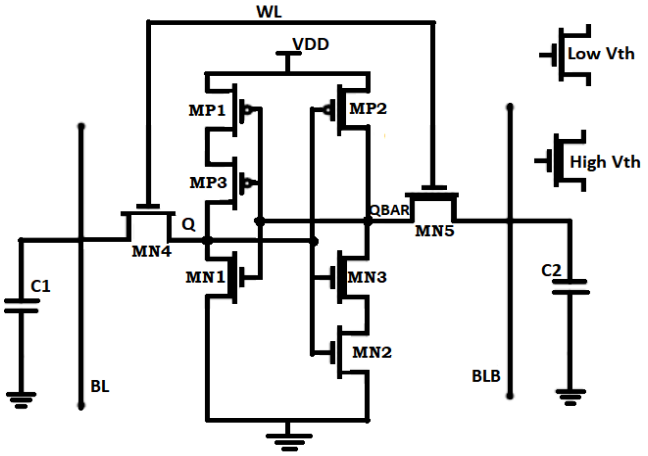


Figure 3: Asymmetric Threshold Stacked CNTFET SRAM Cell

Each CNTFET in the cell is defined by its chirality vector (n, 0) and the number of tubes, which directly influences its threshold voltage Vth and drive strength. The Table 2 outlines the design parameters of each transistor:

Table 2: AT-S CNTFET SRAM Cell Design Configuration

Transistor	Chirality (n)	Number of Tubes	Function
MP1	22	1	Load PCNTFET (pull-up)
MP3	22	1	Load PCNTFET (pull-up)
MP2	19	1	Load PCNTFET (pull-up)
MN1	19	3	Driver NCNTFET (pull-down)
MN3	19	3	Driver NCNTFET (pull-down)
MN2	22	3	Access NCNTFET
MN4	22	3	Access NCNTFET

Note: Lower chirality (n) → Higher Vth; More tubes → Higher drive current.

The Asymmetric Threshold Stacked (AT-S) technique significantly reduces leakage in NVSRAM cells by leveraging strategic transistor sizing, threshold voltage assignment, and device stacking [19]. This approach is explored in CMOS technology, extended to NVSRAM cells, and its potential in Carbon Nanotube Field-Effect Transistor (CNTFET) designs is highlighted.

3.1 AT-S SRAM Cell in CMOS

Figure 3, depicting a Proposed Asymmetric Threshold Stacked SRAM Cell, illustrates an 8T SRAM cell, an advancement over traditional 6T designs for enhanced stability and leakage reduction with its read and write operation depicted in Figure 4.

a) **Asymmetric Thresholds:** This core concept utilizes transistors with different threshold voltages (Vth). High Vth transistors (e.g., MP1, MP2, MN1, MN2 in the feedback path) minimize static leakage in the OFF state, reducing standby power. Conversely, Low Vth transistors (e.g., access transistors MN4, MN5) enable faster switching speeds in the ON state.

b) **Stacked Configuration:** The "Stacked" aspect involves placing transistors in series. When multiple transistors are stacked and OFF, their combined leakage is significantly lower than a single OFF transistor due to the "stack effect," which effectively increases their threshold voltage. In Figure 1, the stacked arrangement within the inverters (e.g., MP1/MP3 and potentially MN1/MN2/MN3) creates longer, higher-resistance leakage paths, particularly effective against subthreshold leakage. The AT-S technique in the basic SRAM cell balances high operating speed during active modes (via low Vth access transistors) with drastic static leakage reduction in standby (via high Vth transistors and stacking in the cell's core).

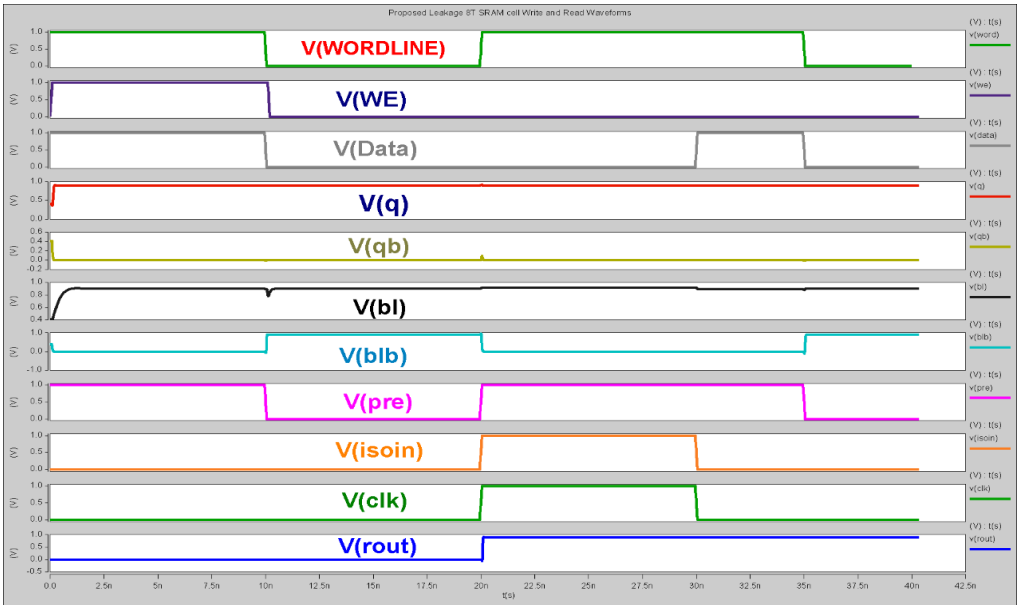


Figure 4: Read and Write Operations Waveforms of Asymmetric Threshold Stacked SRAM Cell

c) **Extending AT-S to NVSRAM for Enhanced Leakage Reduction:** Figures 5, 6, 7, and 8 show how the AT-S SRAM cell is augmented into a Non-Volatile SRAM cell by integrating resistive memory elements (R1, R2, R3 – likely memristors or RRAM) and Leakage Reduction Technique.

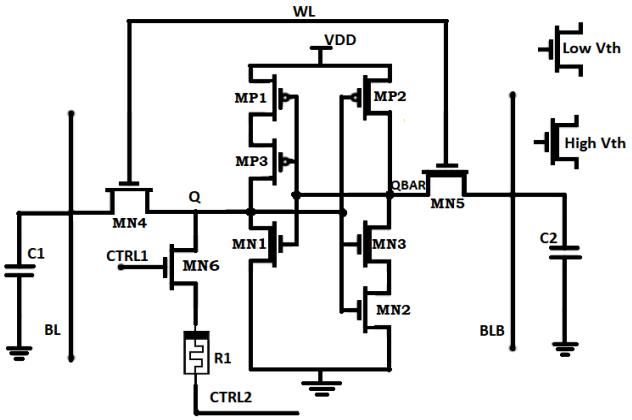


Figure 5: 7T1R NVSRAM Cell With Proposed Leakage Reduction Technique

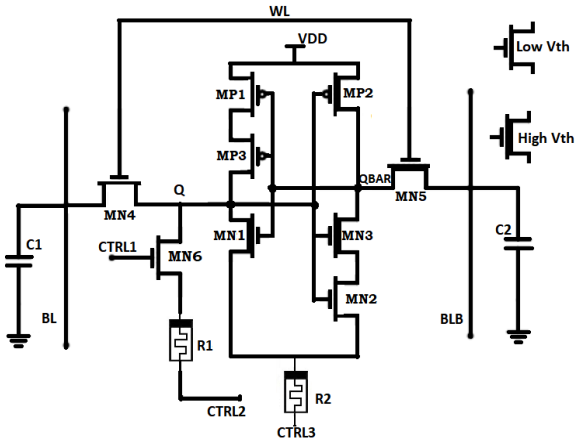


Figure 6: 7T2R NVSRAM Cell With Proposed Leakage Reduction Technique

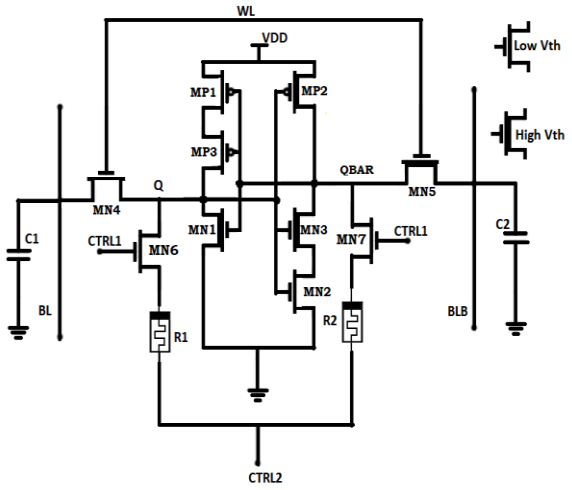


Figure 7: 8T2R NVSRAM Cell With Proposed Leakage Reduction Technique

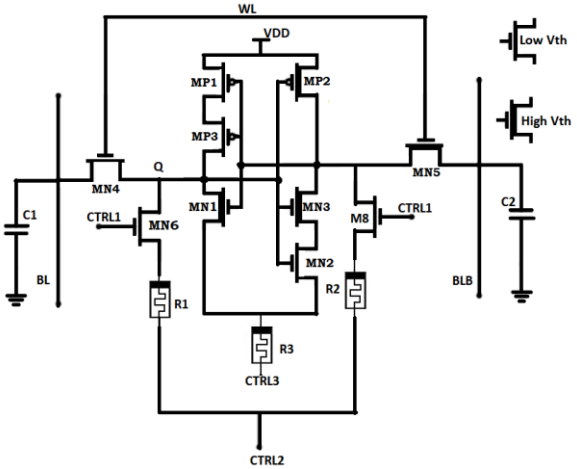


Figure 8: Proposed 8T3RNVSRAM Cell With Proposed Leakage Reduction Technique

d) **Integration of Non-Volatile Elements:** NVSRAM cells incorporate resistive elements parallel to parts of the SRAM latch for non-volatile data storage. Data is saved from volatile SRAM nodes (Q, QBAR) to these elements before power-down and restored upon power-up [20].

Dedicated Leakage Reduction Mechanism: Beyond the intrinsic AT-S of the SRAM core, the Proposed Leakage Reduction Technique involves:

Footer Transistors (MN6, MN7): These NMOS transistors are placed between the SRAM inverters' pull-down network and ground. In the diagrams, MN6 and MN7 connect to Q/QBAR and CTRL2, effectively disconnecting the path to ground.

Control Signals (CTRL1, CTRL2, CTRL3): These signals gate MN6 and MN7. When these transistors are turned OFF (e.g., by CTRL1/CTRL2), they sever leakage paths, significantly reducing static power during standby or data retention. This acts as a cell-level power gating mechanism.

Memristor Gating: The memristors (R1, R2, R3) and their control signals (CTRL2, CTRL3) manage store/recall operations and can also power-gate the non-volatile elements to eliminate their leakage during power-off.

The 7T1R cell (7 transistors, 1 resistive element) and 7T2R cell (7 transistors, 2 resistive elements) represent different non-volatile integration densities. Dynamic power management is enabled by CTRL1, which, when low, turns off MN6 and MN7, cutting ground leakage paths.

e) E. Implementing AT-S in CNTFET NVSRAM Cells: The Next Frontier

While the figures use CMOS symbols, the AT-S concept is highly advantageous for CNTFETs.

- **Inherent Advantages of CNTFETs for AT-S:** Precise Threshold Voltage Control: CNTFET Vth can be finely tuned by varying the carbon nanotube's diameter and chirality, offering superior "Asymmetric Threshold" design compared to CMOS multi-Vth processes.
- **High Performance:** CNTFETs exhibit ballistic transport, leading to higher ON-currents and faster switching. Low-Vth CNTFETs can achieve superior drive strengths than CMOS, enhancing NVSRAM speed.
- **Superior Electrostatic Control and Lower Leakage:** The excellent gate control in CNTFETs results in a steeper subthreshold slope and inherently lower OFF-state currents. The "Stacked" effect further magnifies this intrinsic low leakage, drastically reducing overall power consumption.
- **Memristor Integration:** Advancements in CNT-based memristors can further enhance non-volatile capabilities and reduce power consumption during store/recall.

The entire AT-S NVSRAM circuit topology can be realized with CNTFETs, leveraging their benefits for superior power efficiency, speed, and stability, potentially overcoming CMOS scaling limits and leakage challenges.

f) Overall Benefits and Conclusion

The AT-S leakage reduction technique is a robust design methodology for advanced SRAM and NVSRAM. By combining asymmetric thresholds and stacked configurations, it effectively tackles static power dissipation. In CMOS, AT-S offers a practical balance of performance and power. When extended to NVSRAM with dedicated leakage mechanisms, it enables highly efficient data retention and power management.

The migration of AT-S to CNTFET technology holds immense potential. CNTFETs' precise Vth tunability, superior electrostatic control, and inherent low leakage align perfectly with AT-S principles. This synergy could yield NVSRAM cells with dramatically reduced power consumption, higher speeds, and enhanced stability, paving the way for next-generation memory solutions. As CNTFET fabrication matures, AT-S could be a foundational design principle for ultra-low-power, highly reliable non-volatile memories.

4. Results and Discussion

The Asymmetric Threshold Stacked (AT-S) leakage reduction technique, illustrated across various NVSRAM cell designs (Figures 5-8), represents a sophisticated approach to mitigate static and dynamic power consumption. Building from an 8T SRAM core (Figure 3), the technique integrates non-volatile resistive memory elements and dedicated power-gating transistors (MN6, MN7) controlled by external signals (CTRL1, CTRL2, CTRL3). The core AT-S principle involves judiciously assigning different threshold voltages to transistors—high Vth for lower leakage in standby paths and low Vth for faster switching in active paths—and stacking transistors in series to exploit the "stack effect," thereby significantly reducing subthreshold leakage.

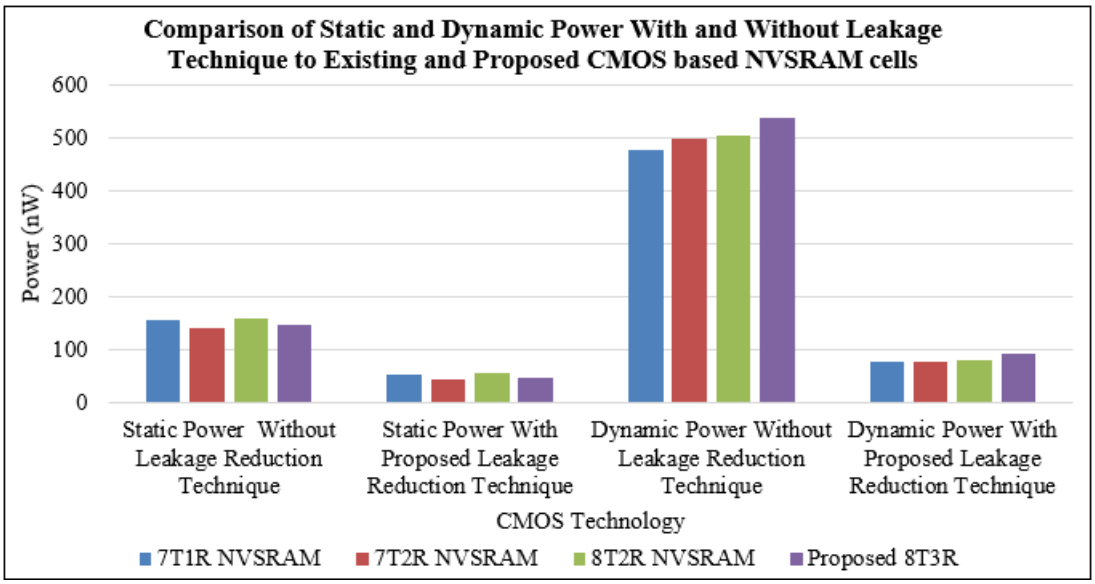


Figure 9: Comparison of Static and Dynamic Power with and without Leakage Technique to Existing and Proposed CMOS based NVSRAM cells Techniques

Simulation results for both CMOS (Figure 9) and CNTFET (Figure 10) implementations strongly validate the efficacy of this technique. In CMOS NVSRAM cells, the AT-S method dramatically cuts static power by over 60%, reducing consumption from approximately 140-155 nW to a mere 40-50 nW A substantial reduction in dynamic power (from ~470-540 nW down to ~70-90 nW) is also observed, highlighting the technique's benefits during active operation. Furthermore, when applied to CNTFET-based NVSRAM, which inherently boasts lower power due to superior electrostatic control and tunable threshold voltages, the AT-S technique achieves even more impressive results. Static power drops from an already low 25-45 nW to an ultra-low 8-15 nW, and dynamic power decreases from 230-270 nW to 55-65 nW

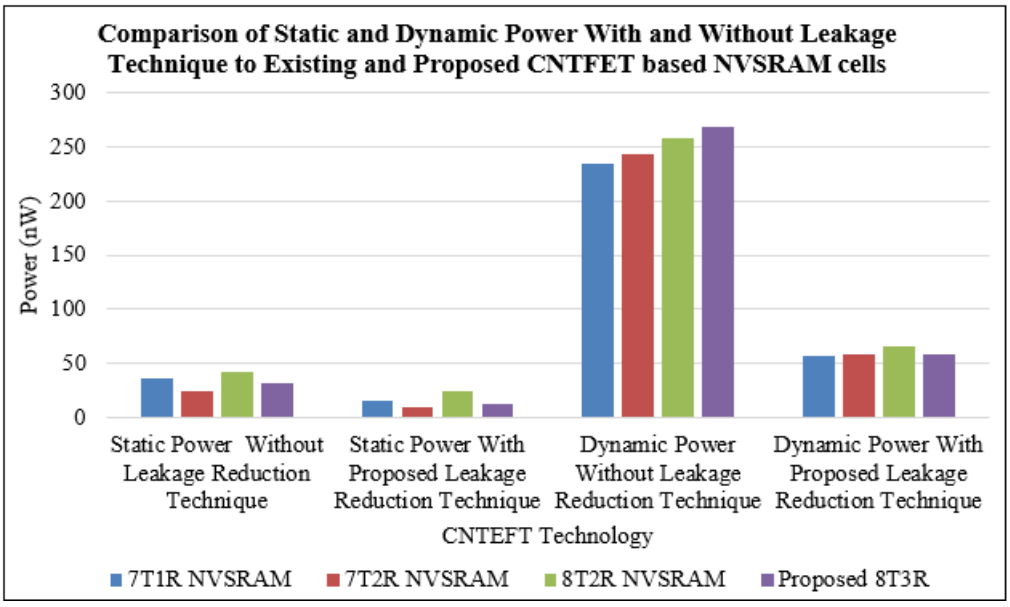


Figure 10: Comparison of Static and Dynamic powers of existing and Proposed Leakage Reduction Techniques

This powerful synergy between the AT-S circuit design and the intrinsic advantages of CNTFET technology underscores its potential for future memory solutions. While slightly higher power figures are noted for more complex cell designs like the Proposed 8T3R variant, the overall impact of the AT-S technique remains profoundly positive. It positions CNTFETs as a leading contender for developing ultra-low-power, high-performance, and highly reliable non-volatile memories, effectively addressing critical power efficiency challenges in advanced electronic systems.

4. Conclusion

This work investigates the design and optimization of NVSRAM cells using CNTFET technology, focusing on minimizing leakage power through the Asymmetric Threshold and Stacking (AT-S) technique. Simulation results show that the AT-S approach achieves up to 69% leakage reduction, significantly enhancing the power efficiency of both conventional and advanced 8T3R NVSRAM designs. The adoption of 16nm CNTFET technology further reinforces the compatibility of the proposed method with modern semiconductor scaling trends. The consistent performance

improvements across multiple NVSRAM configurations underscore the robustness and scalability of the AT-S technique. Overall, the integration of CNTFETs and advanced leakage control strategies like AT-S positions these designs as strong candidates for next-generation, low-power non-volatile memory solutions.

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