International Journal of Scientific Engineering and Research (IJSER)
www.ijser.in
ISSN (Online): 2347-3878
Volume 2 Issue 1, January 2014

Integrated Buck-Buck-Boost AC/DC Converter

Supriya. K[1], Maheswaran. K[2]

[1]M.Tech (Power Electronics & Drives), Department of EEE,
Nehru College of Engineering & Research Centre, Thrissur, Kerala, India

[2]Assistant Professor, Department of EEE,
Nehru College of Engineering & Research Centre, Thrissur, Kerala, India

Abstract: ***Single-Stage transformerless AC/DC converter received much attention in the universal line application. Unlike the existing converters a new high step-down transformerless single-stage single-switch AC/DC converter is proposed. The topology integrates a buck-buck-boost converter with low intermediate bus and output voltage. The converter utilizes a buck converter as a PFC cell and buck-boost converter as a DC/DC cell. The buck-buck-boost converter is able to reduce the bus voltage below 150V under all input and output condition without using a step-down transformer. The absence of transformer reduces the component count, size and cost of the converter. Unlike the existing converter, buck-buck-boost is able to achieve simple control structure with single switch, positive output voltage and high power factor. By using DPT feature, converter is able to achieve high power conversion efficiency. The converter is successfully tested by using MATLAB/Simulink. The simulation result shows that the converter is good tradeoff between reduced bus voltage and high power factor.***

Keywords: Buck-buck-boost converter, power factor correction, single-stage single-switch, transformerless, Direct Power Transfer.

1. Introduction

With the widespread use of power electronics loads, more attention has been given to the power factor correction (PFC) and reducing harmonic distortion in the current drawn from the electric power utility. Moreover, with the stringent modern power quality standards [1], active PFC techniques have rapidly become a vigorous research topic in the power electronics field and considerable efforts have been made on the development of the PFC converters [2], [3].

Active PFC techniques are usually divided into two categories: two-stage and single-stage approaches. The two-stage approach can achieve good performance such as high power factor, low voltage stress and tight output voltage regulation [4]. The major drawbacks of the two-stage approach are its high cost, low power density, low conversion efficiency and complex control, particularly in low-power applications. To overcome these drawbacks, many single-stage PFC topologies have been recently proposed [5].

Single-Stage (SS) ac/dc converters have received much attention in the past decades because of its cost effectiveness, compact size and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [6]-[10]. Their intermediate bus voltage is usually greater than the input line voltage and easily goes beyond 450 V at high-line application. Therefore a bulky capacitor and high-voltage-rating semiconductors have to be used; this increases both the size and cost and will result in lower efficiency [11].

In an effort to reduce the dc voltage on the energy storage capacitor, a number of techniques have been introduced. However, most of the proposed techniques usually comprise of a boost converter for PFC followed by a DC-DC converter for output voltage regulation. With a simple step-down DC-DC cell (buck or buck-boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [12], [13].

A high step-down transformer is usually employed even when galvanic isolation is not mandatory. But leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14]-[16]. In [13], [18] and [19], the converters employ a buck-boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [19] and [13] process power at least twice resulting in low power efficiency. Moreover, the reported converters in [17] consist of two active switches leading to more complicated gate control.

The converter in [20] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. The converter operating with narrow duty cycle, this greatly increases the difficulty in its implementation due to the minimum on time of pulse-width-modulation (PWM) IC.

In this paper, a new power factor correction technology is proposed. The converter formed by two converters namely, a

buck converter as a PFC cell and a buck-boost converter as a DC-DC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. So a transformer is not needed to obtain the low output voltage.

Thus the converter is able to achieve:

1. Low intermediate bus and output voltages in the absence of transformer
2. Simple control structure with a single-switch
3. Positive output voltage
4. High conversion efficiency due to part of input power is processed once and
5. Input surge current protection because of series connection of input source and switch.

Buck-Buck-Boost (BuBuBo) converter circuit configuration and principle of operation is presented in Section II. Design consideration is illustrated in section III. Simulation result of buck-buck-boost converter is given in section IV. Finally conclusion is stated in section V.

2. Circuit Configuration and Principle

The Integrated BuBuBo converter which consists of a buck PFC cell $(L_1, S_1, D_1, C_0 \text{ and } C_B)$ and a buck-boost dc/dc cell $(L_2, S_1, D_2, D_3, C_0 \text{ and } C_B)$ is illustrated in Figure 1 (a). Here L_2 is on the return path of the buck PFC cell, it does not contribute to the cell electrically. Thus L_2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0. Main advantages of DCM operation are:

1. Inherent PFC capability with zero-current switch turn ON
2. Reduction of the reverse recovery problem of the fast diodes in the circuit
3. Good and fast regulation of the output voltage
4. Low-cost power supply can be achieved because of its simplified control circuits

Due to the characteristic of buck PFC cell, there are two operating modes in this circuit. Buck converter operates only when input voltage is greater than output bus voltage.

ModeA(Buck-Boost Mode—V_{in} (θ)≤V_B + V_0): When the input voltage V_{in} (θ) is smaller than the sum of intermediate bus voltage V_B , and output voltage V_0 , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage. Only the buck–boost dc/dc cell sustains all the output power to the load. So two dead-angles $(0-\alpha)$and $(\beta-\pi)$ are present in a half-line period and no input current is drawn as shown in Figure 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Figure 2 (a), (b) and (f). Figure 3(a) shows its current waveforms.

1. Stage 1(d_1T_S): Initially capacitor C_B if fully charged. When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B in the capacitor C_B, while diode D_2 is conducting. Thus the current flows from C_B, L_2, S_1, and D2 to C_B. Output capacitor C_0 delivers power to the load.
2. Stage 2(d_2T_S): When switch S_1 is turned OFF, diode D_3 becomes forward biased and thus energy stored in inductor L_2 is discharged through capacitor C_0 and load R_L.
3. Stage 3(d_3T_S-d_4T_S): The inductor current i_{L2} is totally discharged through C_0 & R_L and C_0 sustains the load current i_0.

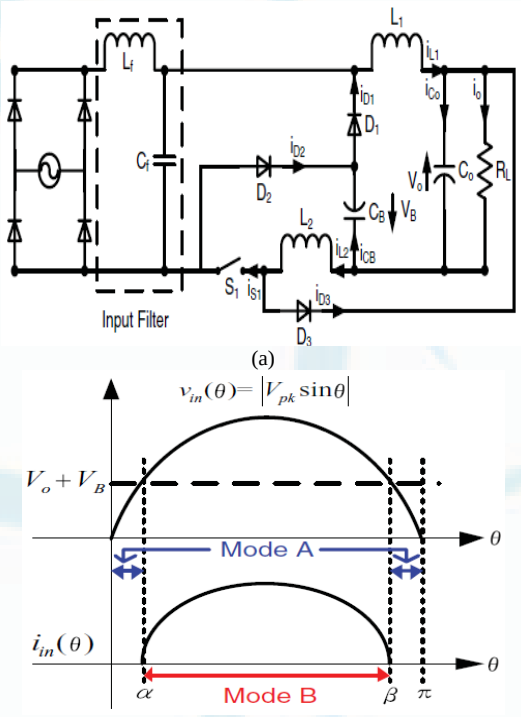

Figure 1: (a) Integrated buck-buck-boost converter (b) Input voltage and current waveforms

Mode B (Buck Mode—V_{in} (θ) > V_B + V_0): In this mode, when the input voltage is greater than the sum of intermediate bus voltage and output Voltage, buck PFC cell get activate. Buck converter operates in the conduction region in between α and β. The circuit operation over a switching period can be divided into four stages. The corresponding circuit is Figure 2(c), (d), (e) and (f). The waveforms are shown in Figure 3(b).

1. Stage 1 (d_1T_S): In this stage when switch S_1 is turned ON, then both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($V_{in}(\theta)$ - V_B - V_0). Here diode D_2 is conducting so capacitor C_B also charged linearly.
2. Stage 2 (d_2T_s): In this stage switch S_1 is turned OFF. Inductor current I_{L1} discharges linearly to C_B and C_0 through D_1, as well as a part of input power is directly fed to the load. At the same time energy stored in the inductor

L_2 is released to C_0 and current is supplied the load through diode D_3. The stage ends once the inductor L_2 is fully discharged.

3. Stage 3(d_3T_S): Inductor L_1 continues to deliver current to C_0 and the load until its current reaches zero.
4. Stage 4(d_4T_S): Only C_0 delivers the output power to R_L.

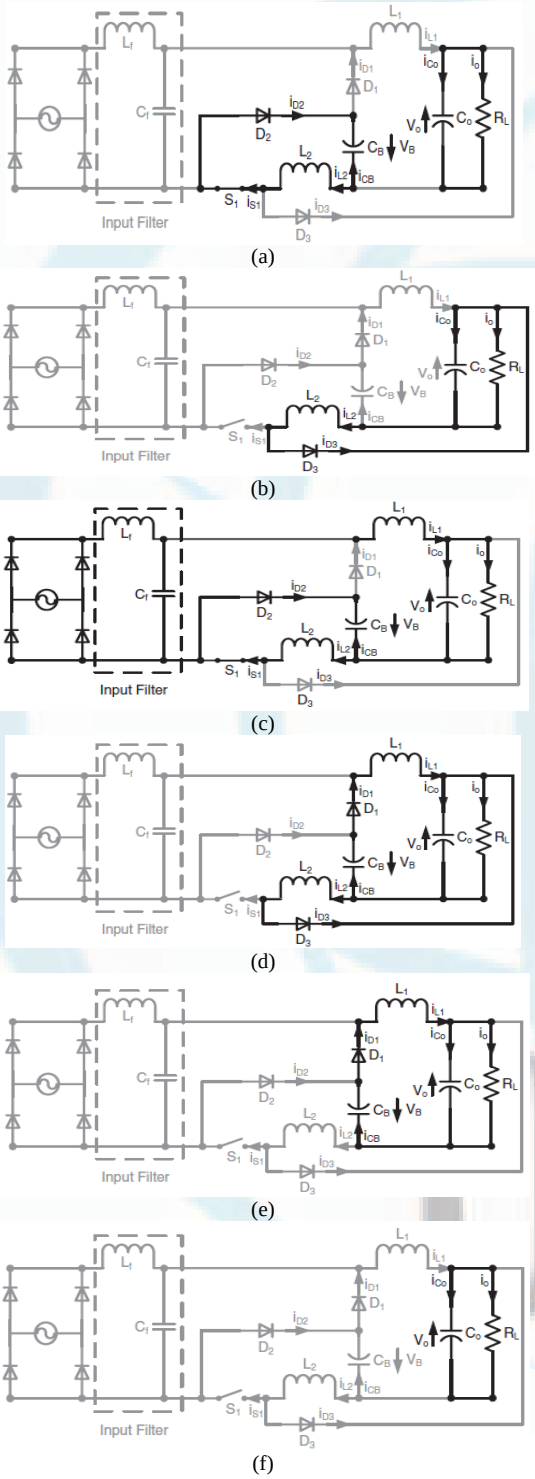

Figure 2: Circuit operation stages of the buck-buck-boost ac/dc converter

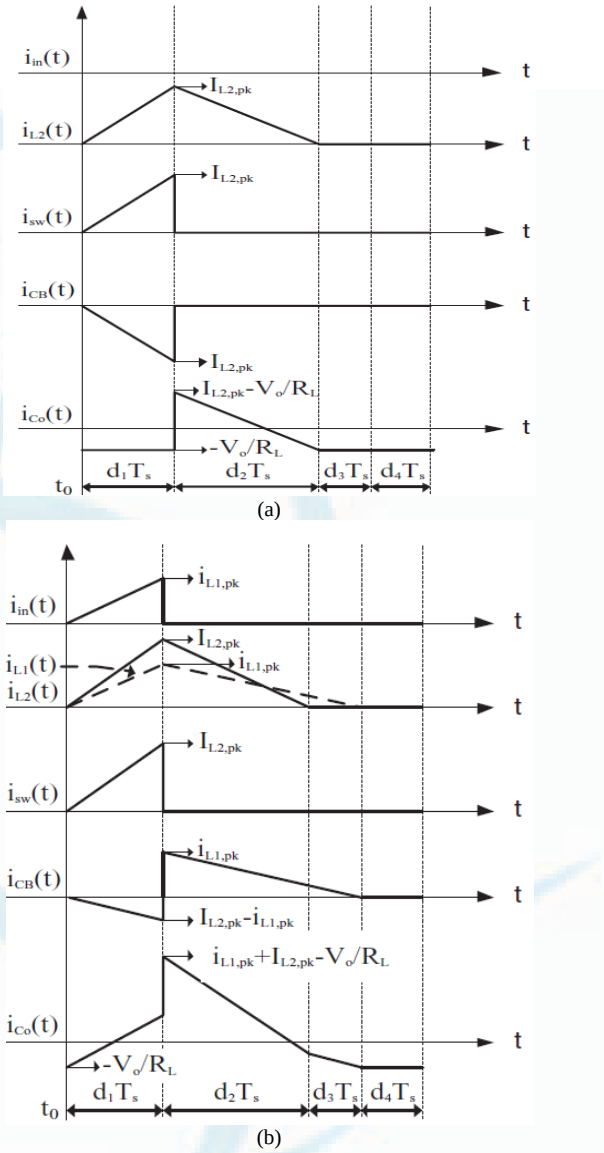

Figure 3: (a) Key waveforms of buck-boost converter (b) Key waveforms of buck converter

3. Design Considerations

Some assumptions are taken to simplify the circuit analysis, they are:

1. All circuit components are ideal.
2. Input voltage $V_{in(\theta)} = V_{pk} \sin\theta$.
3. Both capacitors C_B and C_0 are large so that both capacitors can be treated as constant DC voltage source without ripples.
4. Switching frequency F_s is much higher than input line frequency f.

Here filter capacitor and inductor are used to average the input current. Let consider resonance frequency F_r as 2500Hz. Value of inductor and capacitor is calculated by the equation:

$$F_r = \frac{1}{2\pi\sqrt{L_f C_f}} \qquad (1)$$

Depending on the application, the bulk capacitance value required could be dictated by voltage ripple requirement, hold-up requirements etc. The value of bus capacitance can be calculated from the relation:

$$C_B = \frac{2 \times P_{out} \times t_{hold-up}}{V_{B-no\min al}^2 - V_{B-\min}^2} \qquad (2)$$

P_{out} - Output power in Watt

$t_{hold-up}$ - Hold-up time

$V_{B\text{-}nominal}$ - Nominal bus voltage calculated by iteration

$V_{B\text{-}min}$ - Minimum permissible bus voltage ($\pm$ 6%)

Here both cells operating in DCM mode throughout the ac line period. Thus it must determine critical values of L_1 and L_2 such that, both cells operates in DCM when the inductor values are less than their critical values. The critical inductances are calculated by using the relation:

$$L_{1-crit} = \frac{R_{L-\min} T_S V_{pk} d_{1-\max}^2}{2 \times \pi \times V_0^2} \left[V_{pk} \left(\frac{\gamma}{2} + \frac{A}{4} \right) + V_T \times B \right] \qquad (3)$$

$$L_{2-crit} = \frac{R_{L-\min} V_B^2 T_S}{2V_0^2} d_{1-\max}^2 \qquad (4)$$

Where,

$$V_T = V_B + V_0 \qquad (5)$$

$$A = \sin 2\alpha - \sin 2\beta \qquad (6)$$

$$B = \cos\alpha - \cos\beta \qquad (7)$$

$$d_{1-\max} = \begin{cases} \min(d_{1-PFC}, d_{1-DC/DC}), & \alpha < \theta < \beta \\ d_{1-DC/DC}, & otherwise \end{cases} \qquad (8)$$

$$\gamma = \beta - \alpha \qquad (9)$$

Let $R_{L\text{-}min} = 100\Omega$

$V_0 = 80V$

The output filter capacitance should be selected in order to reduce the ripples presented in the output voltage. The value of capacitance is calculated by using the relation:

$$C_0 = \frac{1}{4 f R_L} \left[1 + \frac{1}{\sqrt{2 Ripplefactor}} \right] \qquad (10)$$

R_L- Load resistance in Ω

f- Line frequency

Ripple factor – It is necessary to reduce ripples present in the output voltage, (1-5) % Ripples

For designing it is necessary to take maximum value of input voltage, take $V_{pk} = 270V_{rms}$

Table 3: Simulation Parameters of Buck-Buck- Boost Converter

Input Voltage	230V rms
Output Voltage	80V
Filter Inductance	2mH
Filter Capacitance	2µF
Inductance L_1	106µH
Inductance L_2	30µH
Bus capacitance C_B	5mF
Output capacitance C_0	5mF
Load resistance R_L	100Ω
Switching frequency	20kHz
Switch type	MOSFET

4. Simulation Results

Simulation circuit for a buck-buck-boost converter with input voltage 230V rms and output voltage of 80V DC is shown in Figure 4. The circuit components are selected in according to the relation (1)-(9) and are listed in the table 1.

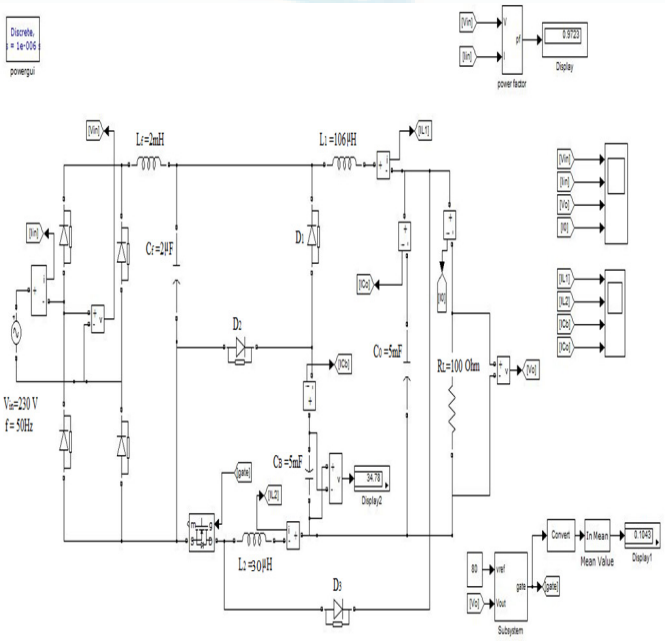

Figure 4: Simulation model of buck-buck-boost converter

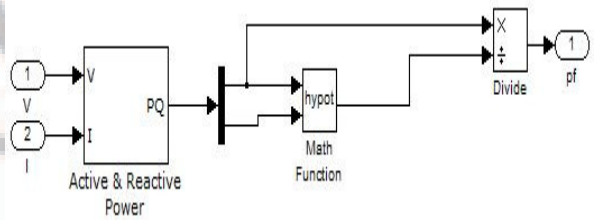

Figure 5: Simulation model of PFC block

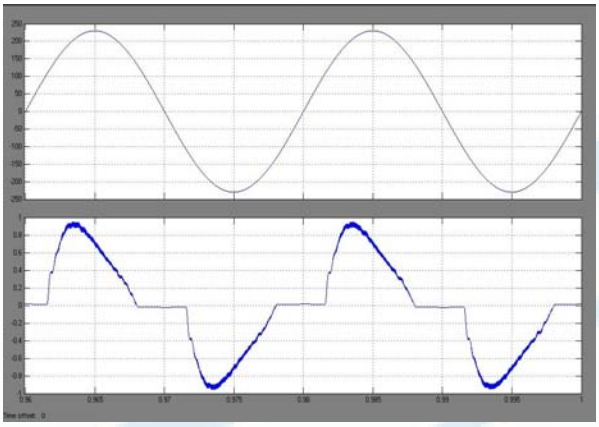

Figure 6: Input current and voltage waveforms of buck-buck-boost converter

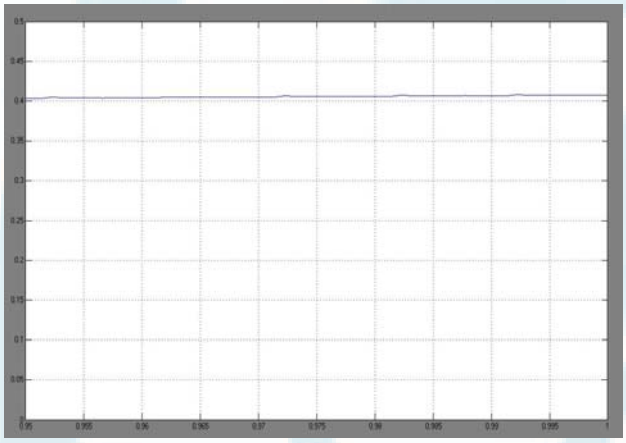

Figure 7: Total harmonic distortion waveform

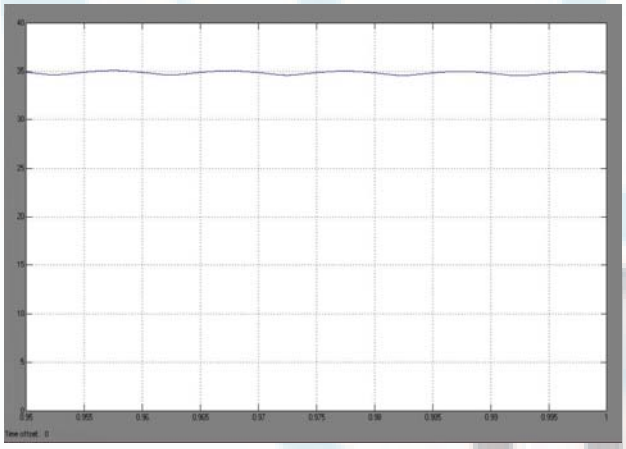

Figure 8: Intermediate voltage waveform of buck-buck-boost converter

Analysis:
1) The total harmonic distortion was obtained as 41%
2) The power factor was obtained as 0.97
3) Intermediate bus voltage was obtained as 35V which is less than 150V

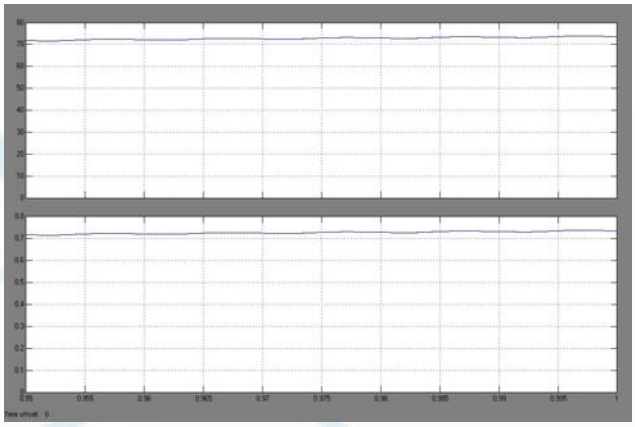

Figure 9: Output current and voltage waveforms of buck-buck-boost converter

5. Conclusion

The Integrated Buck-Buck-Boost single-stage AC/DC converter has been verified experimentally by using MATLAB/Simulink. Buck-Buck-Boost converter is very useful for all universal line application. By using this converter, it is able to achieve bus voltage below 150V at all input and output conditions. So the converter can able to achieve less bus voltage and output voltage without using any resonant converters, high step transformers etc. Thus unlike all the existing converters, Buck-Buck-Boost converters can reduce the component count and complexity in control. Reduced bus voltage allows using low voltage intermediate capacitor. By using Buck-Buck-Boost converter, it is able to achieve a power factor around 0.97. Thus the converter can meet IEC 61000-3-2 standard.

References

[1] International Electro technical Commission, Electromagnetic compatibility (EMC)-Part 3-2: Limits-Limits for harmonic current emissions (equipment input current up to and including 16 A per phase), 3rd ed., IEC 61000-3-2 consolidated edition, Nov. 2005.
[2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, “A review of single-phase improved power quality AC DC converters,” IEEE Trans. Ind. Electron., vol. 50, no. 5, pp. 962–981,Oct. 2003.
[3] R. Ghosh and G. Narayanan, “A Single-phase boost rectifier system for wide range of load variations,” IEEE Trans. Power Electron., vol. 22, no. 2, pp. 470–479, Mar. 2007.
[4] Q. Zhao, F. C. Lee, and F.S. Tsai, “Voltage and current stress reduction in single-stage power-factor correction AC/DC converters with bulk capacitor voltage feedback,” IEEE Trans. Power Electron., vol. 17, no. 4, pp. 477–484, Jul. 2002.
[5] O. Garcia, J. A. Cobos, R. Prieto, P. Alou and J. Uceda, “Single phase power factor correction: A survey,” IEEE Trans. Power Electron., vol. 18, no. 3, pp. 749–755, May 2003.

[6] S. Luo,W. Qiu,W.Wu, and I. Batarseh, "Flyboost power factor correction cell and a new family of single-stage AC/DC converters," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 25–34, Jan. 2005.
[7] D. D. C. Lu, H. H. C. Lu, and V. Pjevalica, "A Single-Stage AC/DC converter with high power factor, regulated bus voltage, and output voltage," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 218–228, Jan. 2008.
[8] M. K. H. Cheung, M. H. L. Chow, and C. K. Tse, "Practical design and evaluation of a 1 kW PFC power supply based on reduced redundant power processing principle," IEEE Trans. Ind. Electron., vol. 55, no. 2, pp. 665–673, Feb. 2008.
[9] D. D. C. Lu, H. H. C. Iu, and V. Pjevalica, "Single-Stage AC/DC Boost: Forward converter with high power factor and regulated bus and output voltages," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2128–2132, Jun.2009.
[10] H.-Y. Li and H. C. Chen, "Dynamic modeling and controller design for a single-stage single-switch parallel boost-flyback–flyback converter," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 816–827, Feb. 2012.
[11] R. Redl and L. Balogh, "Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage," in Proc. IEEE Appl. Power Electron. Conf. Expo., 1995, vol. 1, pp. 454–458.
[12] L. Antonio, B. Andrs, S. Marina, S. Vicente, and O. Emilio, "New power factor correction AC-DC converter with reduced storage capacitor voltage," IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 384–397, Feb. 2007.
[13] E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Buck–boost-type unity power factor rectifier with extended voltage conversion ratio," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1123–1132, Mar. 2008.
[14] Badin and I. Barbi, "Unity power factor isolated three-phase rectifier with two single-phase buck rectifiers based on the scott transformer," IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2688–2696, Sep. 2011.
[15] Abramovitz and K. M. Smedley, "Analysis and design of a tapped inductor buck–boost PFC rectifier with low bus voltage," IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2637–2649, Sep. 2011.
[16] J. M. Alonso, M. A. Dalla Costa, and C. Ordiz, "Integrated buck-flyback converter as a high-power-factor off-line power supply," IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1090–1100, Mar. 2008.
[17] K. Nishimura, K. Hirachi, S. Komiyama, and M. Nakaoka, "Two buck choppers built-in single phase one stage PFC converter with reduced DC voltage ripple and its specific control scheme," in Proc. IEEE Appl. Power Electron. Conf. Expo., 2008, pp. 1378–1383.
[18] T. J. Liang, L. S. Yang, and J. F. Chen, "Analysis and design of a single phase ac/dc step-down converter for universal input voltage," IET Electro. Power Appl., vol. 1, no. 5, pp. 778–784, Sep. 2007.
[19] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Integrated buck–boost–quadratic buck PFC rectifier for universal input applications," IEEE Trans. Power Electron., vol. 24, no. 12, pp. 2886–2896, Dec. 2009.
[20] X. Qu, S.-C. Wong, and C. K. Tse, "Resonance-assisted buck converter for offline driving of power LED replacement lamps," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 532–540, Feb. 2011.

Author Profile

Supriya K received B.Tech degrees in Electrical and Electronics Engineering from College of Engineering Thrikaripur, Kerala in 2011. She is now studying M.Tech in Power Electronics and Drives from Nehru College of Engineering and Research Centre during 2012-2014.

Maheswaran K received ME Degrees in Power Electronics and Drives and BE degrees in Electrical and Electronics Engineering from PSNA college of engineering and research centre Dindigul, Tamil Nadu during the years of 2008-2010 and 2004-2008. He is currently working as an Assistant Professor in Nehru College of Engineering and Research Centre, Thrissur, Kerala.