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Design of Battery-Super Capacitors Combination in Uninterruptible Power Supply (UPS)

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Abstract: ***This paper presents a study of the reduction in battery stresses by using Super capacitors (SCs) in UPS. We aim at investigating the optimal Super capacitors-battery combination versus the SCs cost. This investigation is threefold; first, super capacitors and battery models developed using MATLAB/ Simulink are presented and validated. Second, the architecture and the simulation of the designed system that combines the SCs and the battery are shown. The Super capacitors are used as high-power storage devices to smooth the peak power applied to the battery during backup time and to deliver full power during short grid outages. By charging the SCs through the battery at a suitable rate, all impulse power demands would be satisfied by the Super capacitors. Third, extensive simulations are carried out to determine the gain in battery RMS current, the gain in energy losses, the energy efficiency and the elimination rate of surge load power. These four performance parameters are determined by simulation and then analyzed.***

Keywords: capacitors, Simulink, power, storage, energy, supply, energy loss

1. Introduction

In many industrial sectors, high reliability power supply is required for critical loads. Uninterruptible power supplies (UPS) are used to improve power quality and guarantee the reliability of backup power. During voltage sags or complete interruptions of the power supply, the energy has to be supplied by local energy storage systems (ESS). Conventional ESS for UPS is basically relying on the choice of good lead-acid batteries. However, there are many disadvantages associated with batteries such as low-power density and limited charge/discharge cycles. Moreover, extracting pulsed power instead of average power from the battery can decrease its lifespan. First, the current variations cause voltage transients that can be interpreted by the low-voltage detection circuit as a discharged battery creating a premature shutdown. Second, the pulsed currents have a higher RMS value, which might cause increasing battery losses. Third, pulsating currents also reduce greatly the battery runtime. A super capacitor is a double-layer electrochemical capacitor that can store thousand times more energy than a typical capacitor. It shares the characteristics of both batteries and conventional capacitors and has an energy density about 20% of a battery. Moreover, they have almost negligible losses and long lifespan. They can process a large number of charge and discharge cycles (several hundred thousand cycles) compared to only a few thousand cycles for lead-acid batteries, and can supply much higher currents than batteries. Batteries are mostly efficient when used to supply low, reasonably steady power levels. Super capacitors are very effective in storing charge for later use. Their leakage rate and series resistance are quite small. We present a power-sharing method between the super capacitors and the lead-acid battery in a 500-kVA rated UPS. Combining super capacitors with battery-based UPS system gives the best of high energy and high-power configurations. The super capacitors ensure the power impulses and reduce high power demands away from the battery during the 10-min backup time. They also deliver the whole load power during outages lasting less than 10 s. The lifetime of the batteries could then be extended. We focus then our study of the reduction in battery stresses by the use of SCs. We aim at investigating the optimal SCs/battery combination with respect to the cost price of super capacitors. This investigation is threefold; first, super capacitors and battery models are developed then validated using MATLAB/Simulink software.

1.1 Existing System

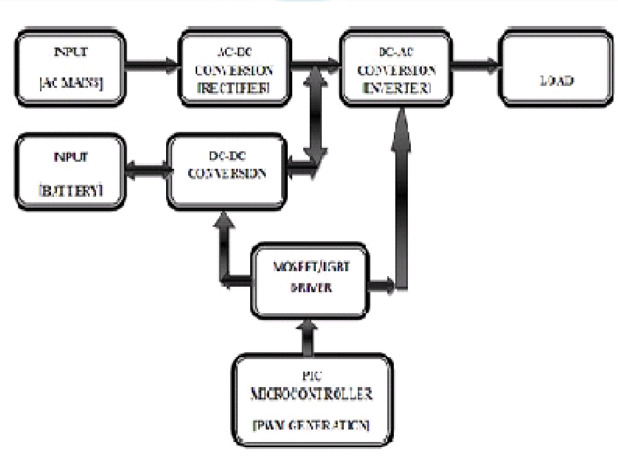

Figure 1: Existing system block diagram

Explanation

Uninterruptible power supplies (UPS) are used to improve power quality and guarantee the reliability of backup power. During voltage sags or complete interruptions of the power supply, the energy has to be supplied by local energy storage systems (ESS).Conventional ESS for UPS is basically relying on the choice of good lead-acid batteries. However, there are many disadvantages associated with batteries such

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as low-power density and limited charge/discharge cycles. Moreover, extracting pulsed power instead of average power from the battery can decrease its lifespan.

1.2 Proposed System

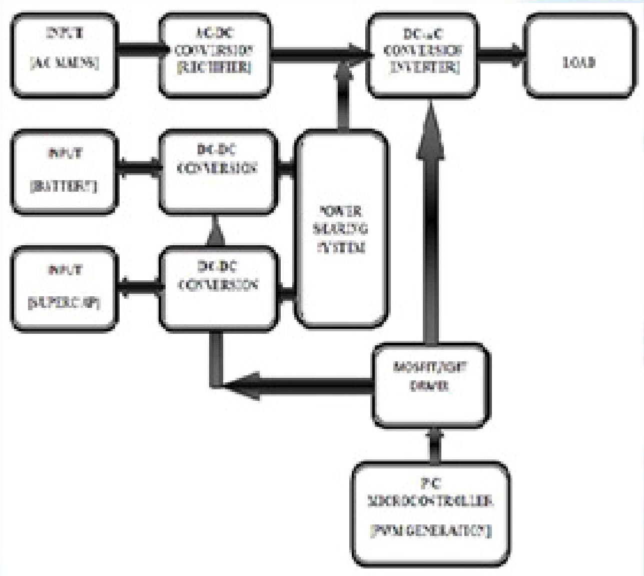

Figure 2: Proposed block diagram

Explanation: Super capacitors are a double-layer electrochemical capacitor that can store thousand times more energy than a typical capacitor. It shares the characteristics of both batteries and conventional capacitors and has an energy density about 20% of a battery. Moreover, they have almost negligible losses and long lifespan. They can process a large number of charge and discharge cycles (several hundred thousand cycles) compared to only a few thousand cycles for lead-acid batteries and can supply much higher currents than batteries. Batteries are mostly efficient when used to supply low, reasonably steady power levels. Super capacitors are very effective in storing charge for later use.

2. Presentation of the Studied UPS

2.1 UPS Specification

Its topology is an Online/Double-Conversion system [2]. Before adding the super capacitors (without the dotted part), in the case of interruption of the power grid rom Input1," the battery supplies immediately the full power to the inverter during short and long outages. The period of backup time is 10 min and it is the required time for the generator to start up and to reach its rated operation. Referring to Standard EN 50160 [3], grid failures requirements are as follows:

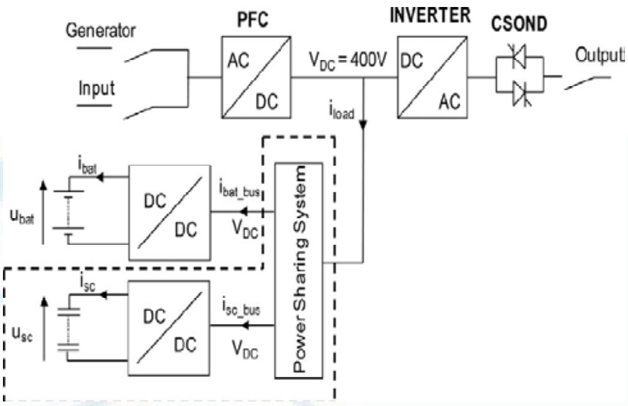

Figure 3: Topology of the 500-kVA UPS

1) Short interruptions of voltage supply: (up to 3 min), few tens–few hundred/year, duration 70% of them <1 s;
2) Long interruptions of voltage supply: (longer than 3 min), <10–50/year.

We mention that in practice, these requirements are not particularly rigorous for the supplier. On the other hand, the consumer regards the limits given in EN 50160 as requirements that must be guaranteed by the supplier [3].

2.2 Super capacitors Pack Sizing and Modelling

We have chosen that the supercapacitors, added as high-power storage devices, must supply the full power P_{load}= P_N during Δt= 10 s, the delivered energy is then estimated to be around 4.8 MJ. The energy E_{sc} stored at the voltage $U_{sc}$of the SCs pack voltage can be expressed as follows:

$$E_{sc} = \frac{1}{2} C_{eq} U_{sc}^2 = \frac{1}{2} \frac{N_{p\_sc}}{N_{s\_sc}} C_{sc} U_{sc}^2$$

Where C_{eq} is the equivalent capaccity of the SCs pack, N_{p_sc} and N^{s_sc} aare the number of the parallel branches and the number of SCs series connections, respectively, and C_{sc} is the SC capacitance. The supercapacitors considered in this pper are the Maxwell/*BCAP3000* type, rated 3000 F, 2.7 V having the parameters given in table 1.

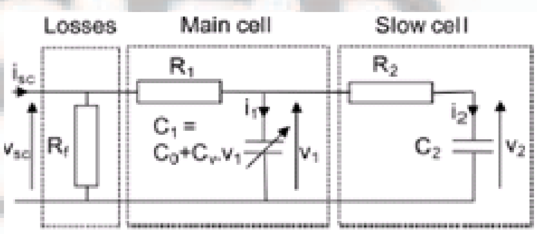

Figure 4: Super-Capacitor simplified circuit: two branches model

It is usually allowed to utilize 75% of the energy stored in the SCs pack by discharging the pack from its rated voltage U_M = 300 V (about 80% of the dc-bus voltage [4] to the half of that value equal to U_m = 150 V. Every elementary SC is then discharged from an initial voltage V_{sci}= 2.7 V to a final voltage V_{scf}= 1.35 V. Further, the internal losses in the SCs

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may be taken into account through the efficiency coefficient $k = 0.9$ [4].

$$P_N \Delta t = k \times \left(\frac{1}{2} C_{eq} U_M^2 - \frac{1}{2} C_{eq} U_m^2 \right).$$

This leads, by considering an energy of 4.8 MJ, to a SCs pack having an equivalent capacitance C_{eq}= 158 F. Referring to the initial voltage of the SCs pack, we obtain $N_{s\ sc}$= 112 and $N_{p\ sc}$= 6. To optimize the super capacitors combination with the battery in UPS applications, we need to establish a model to describe the super capacitor behaviour during fast charge and discharge cycles. We consider the equivalent electric circuit with two RC branches proposed by Zubieta and Bonert [5], Gualous. The main capacitance C_1 (differential capacitance [5]) depends on the voltage v_1 . It consists of a constant capacity C_0 (inF) and a constant parameter C_v(in F/V) and it is written as $C_1 = C_0 + C_v v_1$. The R_1C_1 branch determines the immediate behaviour of the super capacitor during rapid charge and discharge cycles in a few seconds. The R_2C_2 cell is the slow branch. It completes the first cell in long time range in order of a few minutes and describes the internal energy distribution at the end of the charge (or discharge).The equivalent parallel resistance R_f represents the leakage current and can be neglected during fast charge/discharge of the super-capacitor.

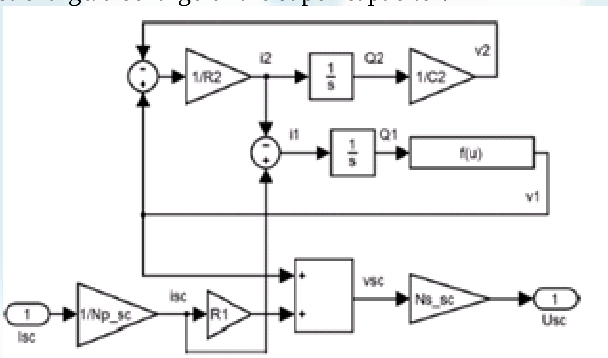


Figure 5: MATLAB simulation model of super capacitors pack

The simulation circuit with MATLAB\Simulink of the super capacitors pack is illustrated. This circuit is based on the following equations (leakage current of super capacitor is neglected):

$$U_{sc} = N_{s\_sc} v_{sc} = N_{s\_sc}(v_1 + R_1 i_{sc}) = N_{s\_sc}\left(v_1 + R_1 \frac{I_{sc}}{N_{p\_sc}}\right.$$

3. Design of Battery - Super Capacitors Combination

3.1 Combination without Control System

First, the battery and the super capacitors have been combined in parallel without control system as shown in Fig.6the dc/dc and the ac/dc converters are supposed to be ideal without losses. The dc-bus voltage V_{DC} is equal to 400 V. The super capacitors are configured as such to have approximately the same total number calculated in the previous section (672 cells) and to ensure initial voltage almost equal to 560 V (OCV battery voltage). We have then $N_{s\ sc}$= 205 and $N_{p\ sc}$= 4.

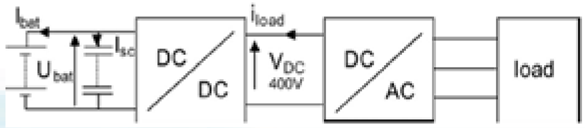


Figure 6: Parallel combination between SCs and battery

3.2 Controlled SCs-Battery Combination

The control system presented in this section is designed to benefit the fast charge and discharge capability of the super capacitors in order to reduce the battery stresses due to instantaneous power demands. The purpose of the combination between SCs and the battery is to make the SCs supply the power transients and to smooth the high-power demands applied to the battery during autonomous operation [8]. Fig 7 shows the new UPS topology counting the control system for power sharing between SCs and the battery.

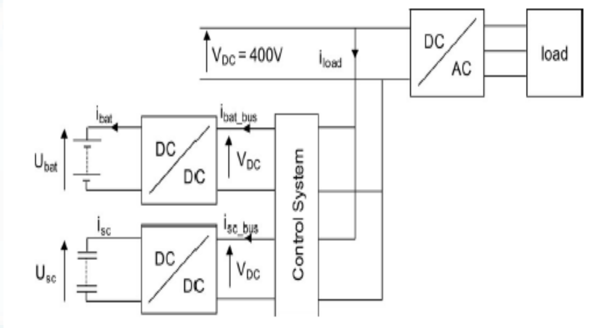


Figure 7: Topology of the controlled SCs/battery combination

The dc/dc converters are supposed to be without losses and modelled as dc ideal bidirectional transformers. The input currents of the converters associated with the battery and the SCs pack, respectively $i_{bat\ bus}$ and $i_{sc\ bus}$ are controlled by the power-sharing system. This control system performs according to the SoC of the SCs pack and to the shape of the load power. The load current i_{load} and the load power P_{load} are distributed to the battery and the SCs according to the principle represented in Fig.6.

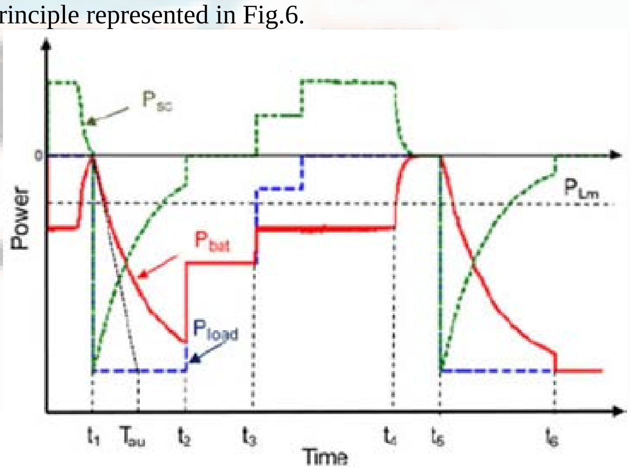


Figure 8: Principle of power sharing between SCs and the battery.

P_{load} is the load power, P_{bat} is the battery power, P_{sc} is the SCs pack power, P_{Lm} is the limit load power, and P_{IV} is the initial value of the battery power.

1) At time t_1, the battery is subjected to a rising power requested by the load. A low-pass filter is applied to the load current diverting sudden power variation to the super capacitors. The equations of this first phase can be written as follows:

$$P_{bat} = P_{load}\left[1 - exp\left(-\frac{t}{T_{au}}\right)\right] + P_{IV}.$$

The SCs power is then given by

$$P_{sc} = P_{load} - P_{bat}.$$

2) The constant Tau characterizes the dynamic of the low pass filter. It is adjustable and can act on the discharge time of the SCs especially on the smoothing degree of the peak power applied to the battery.
3) At time t2, Pload<Pbat, the battery supplies a full load power and the low-pass filter operation is cancelled.
4) At time t3 , the load power Ploadis less than a load power limit PLm, the battery supplies both the load and the SCs pack with energy intended to recharge the super capacitors.

4. Architecture

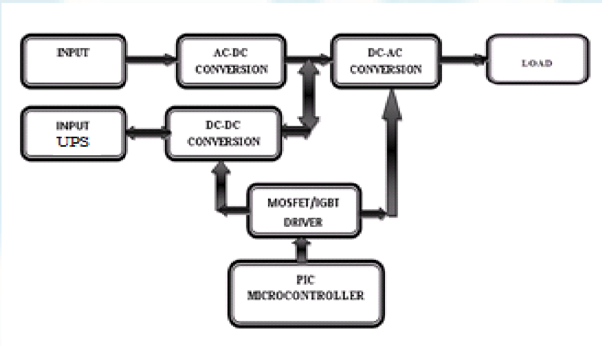


Figure 9: Block Diagram

4.1 Modules

a) Power Electronics Section
   - Diode rectifier, Gate driver circuit, MOSFETs, LC resonant circuit, Filter Capacitor.

b) Microcontroller Section
   - PIC16F877A and PIC16F628A Microcontroller, Keys, LCD, OR logic.
   - PIC16F628A controller is used to compute the efficiency and power factor of the system. It achieves unity power factor when the voltage and current are in phase with each other.

4.2 Flowchart

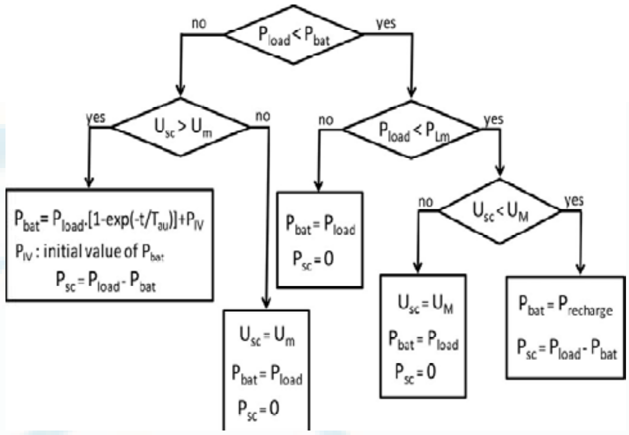
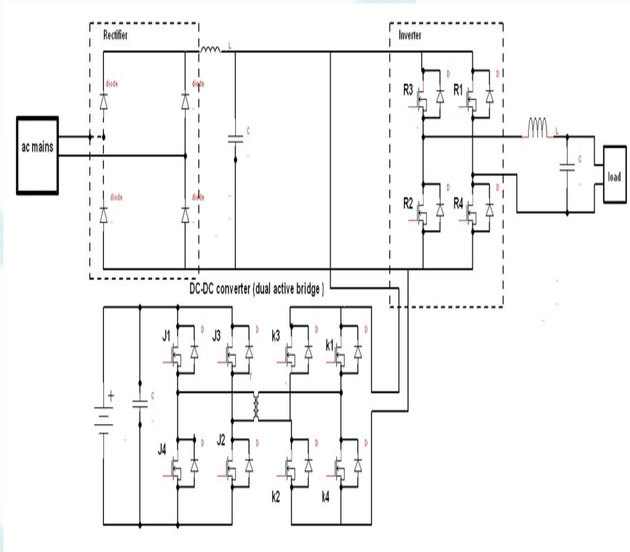


Figure 10: The SC's/battery combination

We examined at the first step the combination of thesuper capacitors with the batter during the UPS backup time of 10 min. A load-power profile, rich in harmonics.

4.3 Circuit Diagram



Explanation

- I present a power-sharing method between the super capacitors and the lead-acid battery in UPS.
- Combining super capacitors with battery-based UPS system gives the best of high energy and high-power configurations
- The Super capacitors ensure the power impulses and reduce high-power demands away from the battery during the 10-min backup time.
- They also deliver the whole load power during outages lasting less than 10 s. The lifetime of the batteries could then be extended.
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- They also deliver the whole load power during outages lasting less than 10 s. The lifetime of the batteries could then be extended.

4.3.1 Circuit Description: Voltage Doubler 12/24 volts

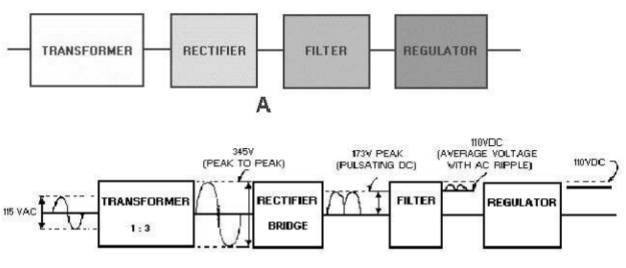
This circuit was born from the requirement to have 24 volts DC in remote 12 volts DC operated boxes, such as microwave transverters or other control units. This was aimed to properly drive relays, fans, etc. operating at 24V. This circuit was replicated in hundred of units operating indoor/outdoor also with extreme conditions of heat/cold very successfully.

The circuit consists in a simple, rugged BF amplifier put to self-oscillate to generate a square wave at 70 KHz circa. Then the square wave is rectified with a voltage doubler consisting of D1, D2, C3 and C4. The TDA2003 is built to deliver some 10 watts of power, the doubled output voltage at 24-26 volts (voltage out is depending by voltage in) it exceeds430mA of current. The TDA2003 output stage works saturated therefore the power dissipated by the IC is quite low. Due to the little dissipation a big heatsink is not needed. Many units were built in a 'dead bug' manner soldering directly the IC dissipator pad onto a small rectangular piece of PC board 2.5cm x 1.5cm acting as a support for the circuit, as well as an heatsink (with full copper on the board obviously). The idling current (no output load) is approximately 40mA.

For D1 and D2 (1 amp at least) fast rectifiers shall be used while C3 and C4 shall better be low ear units; this said, standard caps and diodes were used with success although with slightly diminished performances (voltage and ripple). C3 and C4 values of 330uF are adequate (not critic). Make sure to properly decouple the 12 V power supply by means of ceramic and low esr electrolytic capacitors; on the schematic I put only one 470uF low esr for 'drawing convenience' but it won't hurt to put other ones in parallel as close as possible to the TDA input pin.

4.4 Hardware Used

4.4.1 Micro Controller Power Supply Unit

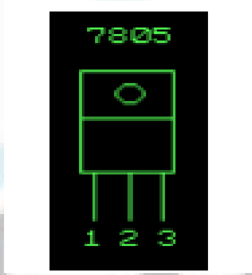


The transformer steps up or steps down the input line voltage and isolates the power supply from the power line. The RECTIFIER section converts the alternating current input signal to a pulsating direct current. However, as you proceed in this chapter you will learn that pulsating dc is not desirable. For this reason a FILTER section is used to convert pulsating dc to a purer, more desirable form of dc voltage.

The final section, the REGULATOR, does just what the name implies. It maintains the output of the power supply at a constant level in spite of large changes in load current or input line voltages. Now that you know what each section does, let's trace an ac signal through the power supply. At this point you need to see how this signal is altered within each section of the power supply. Later on in the chapter you will see how these changes take place. In view B of figure 4-1, an input signal of 115 volts ac is applied to the primary of the transformer. The transformer is a step-up transformer with a turn's ratio of 1:3. You can calculate the output for this transformer by multiplying the input voltage by the ratio of turns in the primary to the ratio of turns in the secondary; therefore, 115 volts ac ´ 3 = 345 volts ac (peak-to- peak) at the output. Because each diode in the rectifier section conducts for 180 degrees of the 360-degree input, the output of the rectifier will be one-half, or approximately 173 volts of pulsating dc. The filter section, a network of resistors, capacitors, or inductors, controls the rise and fall time of the varying signal; consequently, the signal remains at a more constant dc level. You will see the filter process more clearly in the discussion of the actual filter circuits. The output of the filter is a signal of 110 volts dc, with ac ripple riding on the dc.

4.4.2 Circuit Diagram of the Power Supply

The capacitors must have enough high voltage rating to safely handle the input voltage feed to circuit. The circuit is very easy to build for example into a piece of Vero board.



4.4.3 Pin out of the 7805 regulator IC

1) Unregulated voltage in
2) Ground
3) Regulated voltage out

4.4.4 Component List

- 7805 regulator IC
- 100 uF electrolytic capacitor, at least 25V voltage rating
- 10 uF electrolytic capacitor, at least 6V voltage rating
- 100 nF ceramic or polyester capacitor

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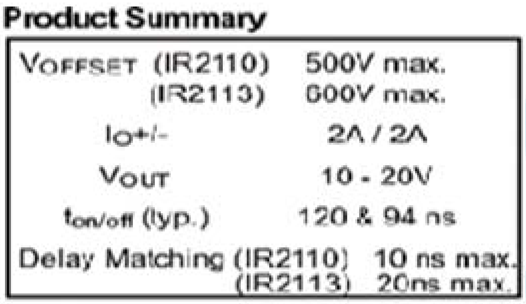
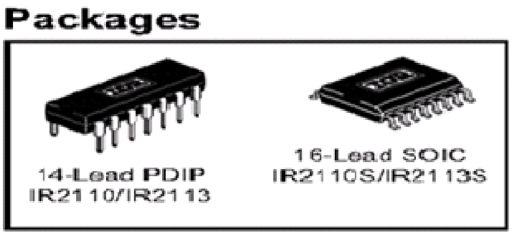
4.4.5 Drive Circuit (IR2110)



Product Summary

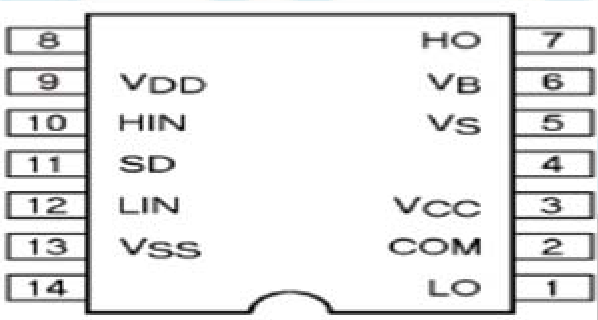
VOFFSET	(IR2110)	500V max.
	(IR2113)	600V max.
Io+/-		2A / 2A
VOUT		10 - 20V
ton/off (typ.)		120 & 94 ns
Delay Matching	(IR2110)	10 ns max.
	(IR2113)	20ns max.

Packages



The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

4.4.6 Pin Configuration



5. Simulation

5.1 General

Simulation has become a very powerful tool on the industry application as well as in academics, nowadays. It is now essential for an electrical engineer to understand the concept of simulation and learn its use in various applications. Simulation is one of the best ways to study the system or circuit behavior without damaging it .The tools for doing the simulation in various fields are available in the market for engineering professionals. Many industries are spending a considerable amount of time and money in doing simulation before manufacturing their product. In most of the research and development (R&D) work, the objective of this chapter is to describe simulation of;

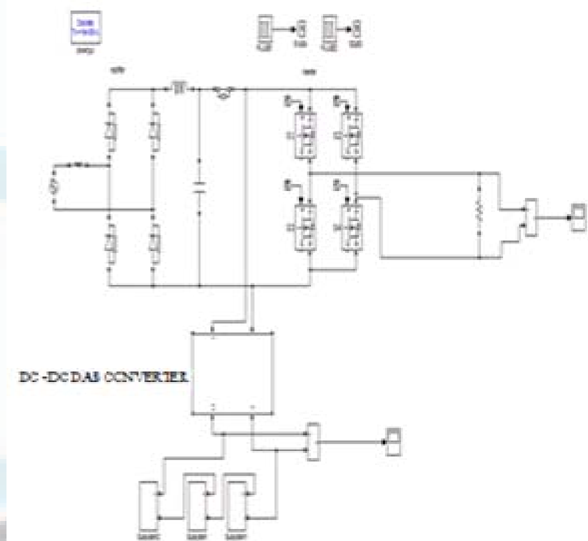
- Impedance source
- Inverter with R, R-L and RLE loads
- Using MATLAB tool.

5.2 Introduction to MATLAB

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. Typical uses include;

1. Algorithm development
2. Data acquisition
3. Modeling, simulation, and prototyping
4. Data analysis, exploration, and visualization
5. Scientific and engineering graphics
6. Application development, including graphical user interface building

5.3 Simulation Diagram



DC-DC DAB converter circuit simulation diagram

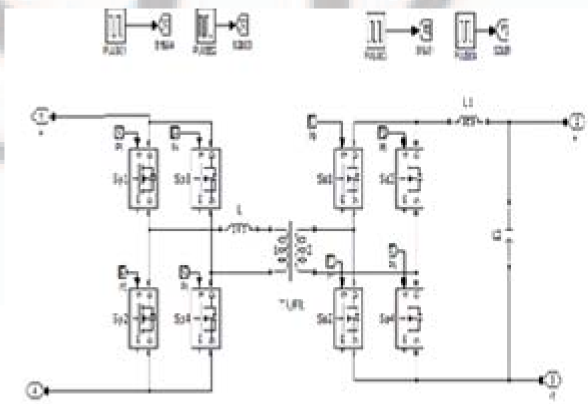


Figure 5.1: Online Circuit Simulation Diagram

5.3 Simulation Output

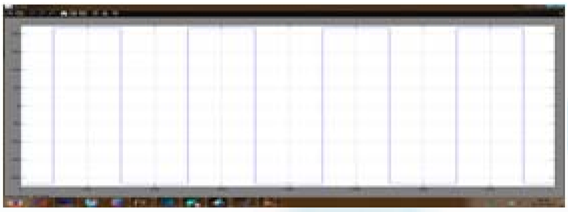


Figure 5.2: Over all voltage output

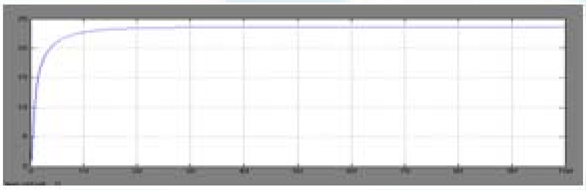


Figure 5.3: Super capacitor output

6. Conclusion

In this paper, the design of a control system that optimizes the battery-supercapacitors combination in a 500-kVA rated UPS has been presented. The advantage of having a hybrid energy source for the UPS has been shown. The importance of supercapacitors in peak-power smoothing has been elaborated on. TheSCs pack and the battery are modelled using MATLAB/Simulink software and then validated. The reduction in battery stresses has been discussed. The supercapacitors overcome the power surges and reduce high-power demands away from the battery during the backup time. They also ensure the whole load power during outages lasting less than 10 s. The study of some performance parameters with respect to the cost of the SCs pack has also been presented and an optimal configuration has been found for a filter constant *Tau* = 2 s, a number of SCs parallel branches *Np sc*=8, and battery recharge current *Ibat charge* = 400 A. The cost of this system is higher today than pure battery system, however, it should be pointed out that supercapacitors undergo intensive development and become more and more available in small size and low price. At the current state, the SCs pack cost is almost triple of the battery pack cost. The system we conceived would be efficient if the battery lifetime is enhanced at least four times. We are undertaking accelerated tests on lead-acid batteries to observe the effect of pulsed loads and smoothed loads on battery wear out process and reliability. Some extensions of this study are undertaken and experimental bench has been set up to carry accelerated tests on lead-acid batteries. We aim to observe the effect of pulsed loads and smoothed loads on battery wear out process and reliability in order to quantify the efficiency of the designed system.

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