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Simulation and Implementation of Digital Controlled Single Phase Transformer Based Inverter for Non-Linear Load Application

N. Devaraj[1], K. S. S. Prasad[2]

[1]PG Scholar, Department of EEE, Bharath University, Bharath Institute of Science and Technology, Selaiyur Chennai-73, India

[2]Assistant Professor, Department of EEE, Bharath Institute of Science and Technology, Bharath University, Selaiyur Chennai-73, India

Abstract: ***This Paper presents Simulation and Implementation of Series-Resonant APWM Converter. It is composed of a generalized analysis for the auxiliary network in a modified series-resonant asymmetrical pulse width-modulated (APWM) converter. Telecommunications and computer systems require power supply topologies frequencies. This is a simple topology that operates at a constant in that offer high efficiency and high power density at ever increasing switch is performed to produce a design procedure ant frequency and with near Zero voltage switching losses. It ensures that zero voltage switching (ZVS) is achieved for any series-resonant APWM converter design. New equations that correctly predict the magnitude of auxiliary current are obtained by accounting for the trapezoidal nature of the waveforms associated with high-frequency operation, and the dead time between the switches in the half-bridge. A prototype of the modified topology is constructed and experimental analysis supports the theoretical results. To further improve the performance the use of MOSFET's as synchronous rectifiers in place of diode rectifiers is proposed. Experimental results verify that ZVS is achieved, and that the proposed design reduces the auxiliary inductor.***

Keywords: APWM-advanced pulse width modulation, converter, ZVS, *MOSFET.*

1. Introduction

This paper **"**Simulation and Implementation of Series-Resonant APWM Converter**"** aimed at obtaining the use Resonant converters have been well documented to meet the requirements of the different resonant tank structures [5]; the series-resonant converter is the simplest structure that has inherent protection against transformer saturation. It promotes high efficiency through ZVS of the primary switching devices [3], ZCS of its rectifiers, and load-dependent current. These features make it attractive at medium to high power levels with one or more full-bridge structures that interface renewable energy sources with loads.

In this Asymmetrical Pulse Width Modulation Control, the gate pulses to the two switches of bridge legs have complementary duty cycles. Therefore, the bridge output voltage has dc component, which needs to be blocked before applying to the RN. In this context, RNs with band pass characteristics, it has been popularly applied to power converters (resonant as well as non-resonant) due to simpler implementation and soft-switching over the wide range of operation [7].

Adding auxiliary circuits composed of multiple semiconductors and passive elements around each power device in standard pulse width modulation (PWM) topologies achieves soft switching with more design effort and increased size and cost. For low power, a single half-bridge structure is required for high power density. Soft-switching PWM converters are an option, but they suffer from loss of ZVS at some operating conditions, and voltage stress that exceeds the input voltage. The latter forces the use of slower, higher on-resistance devices. The series-resonant asymmetric pulse-width-modulated converter (SR-APWM) is a half-bridge load resonant topology that achieves the soft-switching benefits of the series-resonant tank while operating at constant frequency [8] concludes that a dual edge PWM controller was proposed for secondary side control of current type resonant converters operating at constant frequency. It was also shown that high efficiency can be maintained across the load range due to the sinusoidal nature of the resonant current. [1].

It concludes that dead time is a critical factor that influences the entire system design and using through investigation, an optimal design methodology is proposed to achieve high efficiency over a wide load range. An optimal transformer structure for the resonant converter is proposed to achieve low winding loss and to have the capability of magnetic integration and easily implemented. [2]

This chapter deals with the operation principle of Modified series-resonant APWM schematic. In the series-resonant asymmetric pulse-width-modulated converter (SR-APWM) is a half-bridge load resonant topology that achieves the soft-switching benefits of the series-resonant tank while operating at constant frequency. Its resonant inductor can be formed entirely by the transformer leakage inductance to further increase power density. Constant frequency operation simplifies electromagnetic compatibility and magnetic component design. All these benefits make it an ideal candidate for low-voltage, low-power supplies. In

addition to the aforementioned merits, the output filter of the SR-APWM is purely capacitive, thereby enabling it to respond quickly to load transients. Thus, using the SR-APWM as a 48-V voltage regulator (VR) would not only improve system efficiency by reducing the load on the intermediate bus but also provide improved transient performance over the buck converters currently powering microprocessors, and application-specific integrated circuits. However, with the reduction of supply voltages required by high-speed digital circuits, a high transformer turns ratio is required for the SR-APWM. This reduces the reflected load current, which has the benefit of low conduction loss, but potentially leads to a loss of ZVS due to the no idealities of MOSFET devices. To ensure ZVS is achieved, a passive auxiliary network originally applied to the phase-shift-modulated full bridge was applied to the SR-APWM in order to increase its input voltage range. The design procedure presented in presents a trade-off between inductor size and conduction loss.

At high frequency, the dead time required to achieve ZVS constitutes a greater percentage of the switching period, and the charge associated with the output capacitance of the switches cannot be neglected. With present-day high-speed digital devices requiring low supply voltages, and the desire to switch at high frequency, the modified SR-APWM used in 48V VR applications is prone to the two issues discussed previously.

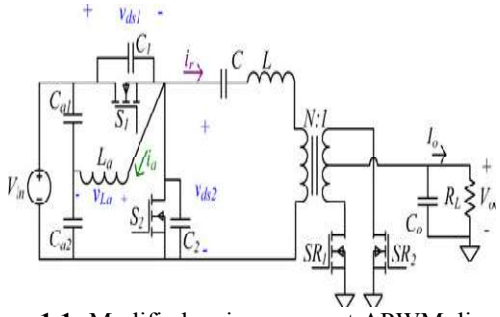


Figure 1.1: Modified series-resonant APWM diagram

It is, therefore, imperative to ensure that generalized equations are available to guarantee proper design. In this project, a more thorough analysis is provided, with the results used for a design procedure based on concurrent design of the resonant tank and auxiliary network. Experimental results are provided, and are shown to correlate well with predicted and simulated values.

2. Steady-State Operation

2.1 Resonant Tank

The resonant tank is excited by a unipolar trapezoidal wave Vds2 created by the chopper formed by complementary switches S1 and S2. The capacitor C resonates with L, and also acts as a dc block to prevent transformer saturation. The sinusoidal resonant current is stepped up by the transformer, rectified by synchronous rectifiers SR1 and SR2 and then filtered by Co. Line regulation is achieved by varying the duty cycle D of S1. Load regulation can also be achieved through varying the primary-side duty cycle or through secondary-side control.

The ac component of Vds2 is represented by a Fourier series expansion given by (1), where fÖ0 is the radian operating (switching) frequency, and n is the harmonic index. The phase angle of the chopper voltage is defined by (2). The magnitude of the impedance of the resonant tank is given by (3), and the associated phase angle by (4). The fundamental of the resonant current defined by (5) is simply the ratio of drive voltage to tank impedance.

$$V_{\mathrm{sn}} = \sum_{n=1}^{\infty} \frac{\sqrt{2}V_{\mathrm{in}}\sqrt{1-\cos\left(2n\pi D_{\mathrm{ch}}\right)}}{n\pi} \sin\left(n\omega_0 t + \theta_n\right)$$

$$\theta_n = \tan^{-1}\left[\frac{\sin\left(2n\pi D_{\mathrm{ch}}\right)}{1-\cos\left(2n\pi D_{\mathrm{ch}}\right)}\right]$$

$$|Z_{\mathrm{eq}}| = R_{\mathrm{ac}}\sqrt{1+Q^2\left(\omega-\frac{1}{\omega}\right)^2}$$

$$\phi = \angle Z_{\mathrm{eq}} = \tan^{-1}\left[Q\left(\omega-\frac{1}{\omega}\right)\right]$$

$$i_{\mathrm{r}}(t) = \frac{|V_{\mathrm{s1}}|}{|Z_{\mathrm{eq}}|}\sin\left(n\omega_0 t + \theta_1 - \phi\right).$$

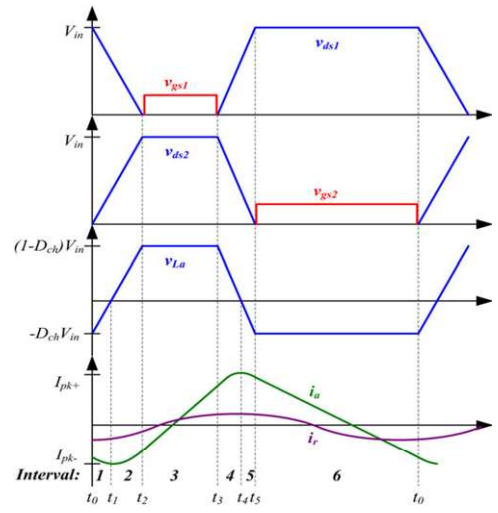


Figure 2.2: Operating waveforms of the Modified SR-APWM converter

In Rac is the equivalent ac resistance of the load and rectifiers referred to the transformer primary. The equation for Rac is given by where RL is the converter load resistance; N is the transformer turns ratio, and fÀ is a conversion factor that is unity under traditional primary-side control methods, and greater than or equal to unity when load regulation is achieved by secondary side control. The resonant frequency of the tank is given by, relative operating frequency by, and quality factor by;

$$R_{ac} = \frac{8N^2\beta}{\pi^2}R_L$$

$$\omega_r = \frac{1}{\sqrt{LC}}$$

$$\omega = \frac{\omega_0}{\omega_r}$$

$$Q = \frac{\omega_r L}{R_{ac}}.$$

As switching frequency is increased, the time necessary to allow the switches to commutate and achieve ZVS becomes a greater portion of the switching cycle, thereby making the assumption that the drain source voltage is a vertical edge inaccurate. The new definition of duty cycle accounting for finite charge time of the drain Source capacitance where T is the switching period, and Tch1 = t2.t0, and Tch2 = t5.t3 are the snubber capacitor charge times

$$D_{ch} = \frac{t_{on}}{T} + \frac{T_{ch1} + T_{ch2}}{2T}.$$

Under APWM control, the voltage conversion ratio is given by, where N is the transformer turns ratio

$$\frac{V_o}{V_{in}} = \frac{\sqrt{1-\cos(2\pi D_{ch})}}{2\sqrt{2}N}\frac{1}{\sqrt{1+Q^2(\omega-(1/\omega))^2}}.$$

The voltage stresses of the resonant elements are proportional to the current flowing through them. The stresses of the capacitor and inductor relative to the fundamental of the chopper voltage are given by (12) and (13), respectively.

2.3 Auxiliary Circuit

The auxiliary circuit operates independent of the resonant tank, and experiences six operating intervals, which are described in the following. The assumption made is that the voltage across the auxiliary capacitors is constant.

1) Interval 1 (t0 > t < t1
This interval begins with switch S2 turning OFF, and its voltage slowly rising to achieve zero voltage turn-off. The rate of rise is limited by the snubber capacitance Csb across the two switches (C1 + C2), which is composed of the output capacitance plus any additional capacitors. The current through the auxiliary inductor decreases, and the interval ends when the voltage across the auxiliary inductor is zero, and the auxiliary current is at its negative peak value

$$I_{pk-} = \frac{-D_{ch}V_{in}}{2L_a}\left[(1-D_{ch})(T-T_{ch1})\right].$$

2) Interval 2 (t1> t < t2):
The voltage across S2 continues to rise and the auxiliary inductor current rises from its negative peak value. The interval ends when the snubber capacitors are fully charged and the voltage across S2 equals the input voltage.

$$i_a(t_2) = \frac{-(1-D_{ch})V_{in}}{2L_a}\left[D_{ch}T + T_{ch1}\right]$$

3) Interval 3 (t2 > t < t3):
S1 is turned ON under zero voltage to begin this interval. The current through La ramps up linearly until S1 is turned OFF at the end of the interval. The value of auxiliary current at t3 can be calculated as

$$i_a(t_3) = \frac{(1-D_{ch})V_{in}}{2L_a}\left[D_{ch}T - T_{ch2}\right]$$

v

4) Interval 4 (t3 >t < t4):
With both switches OFF, the voltage across S2 begins to fall; meaning the voltage across S1 begins to rise. As with switch 2, the rate of rise is limited by the snubber capacitance, so zero-voltage turn-off is achieved. The auxiliary current rises and reaches its positive peak value Ipk at the end of the interval

$$I_{pk+} = \frac{D_{ch}V_{in}}{2L_a}\left[(1-D_{ch})(T-T_{ch2})\right].$$

5) Interval 5 (t4 >t < t5):
In this interval, the voltage across the auxiliary inductor falls from zero, and the auxiliary current falls from its positive peak. The interval ends when the drain. Source voltage of S2 reaches zero. At this instant, the voltage across S1 is equal to the input voltage, and the current through the auxiliary network is found with

$$i_a(t_5) = \frac{D_{ch}V_{in}}{2L_a}\left[(1-D_{ch})T - T_{ch2}\right].$$

6) Interval 6 (t5> t < t0):
Switch 2 is turned ON under zero voltage to begin this interval. With S2 ON, the auxiliary inductor current ramps down linearly. This interval ends when S2 is turned OFF, and the cycle is repeated

$$i_a(t_0) = \frac{-D_{ch}V_{in}}{2L_a}\left[(1-D_{ch})T - T_{ch1}\right].$$

2.4 Design Procedure

2.4.1. Resonant Tank

In low-power, high-frequency applications, the design of the resonant tank is typically a tradeoff between conduction loss and component stress, constrained by the leakage inductance of the transformer. To maintain line regulation, there must be sufficient gain at minimum input voltage. This provides the first constraint of possible circuit configurations. Resonant component stresses are shown in Fig. 2.3 to illustrate the impact of different resonant tank parameters. As shown, high Q implies high stress. Increased $f\ddot{O}$ results in lower stress, but leads to increased circulating current which leads to increased conduction loss.

In Fig. 2.3, the values of the resonant tank current at the instant the switches turn OFF are shown for a given set of tank parameters. For S2 to achieve ZVS, the turn-off current of S1 IS1off has to be positive. For S1 to achieve ZVS, the turn-off current of S2 IS2off must be negative. When $f\ddot{O}$ is increased, the curves shift away from each other and it appears that there is potential for S1 to achieve zero voltage turn-on. However, in practice, the turn-off current of S2 is not large enough to discharge the snubber capacitors, while the turn-off current of S1 has increased. This places competing requirements on the auxiliary network and is actually counterproductive. Traditionally, operating away from the resonant frequency is opted for to increase circulating current and achieve ZVS. With proper design, the increased conduction loss is small compared to the switching loss savings at high frequency. Since the modified series-resonant APWM converter has an auxiliary network to achieve ZVS, circulating current associated with the resonant tank is unnecessary and can be reduced.

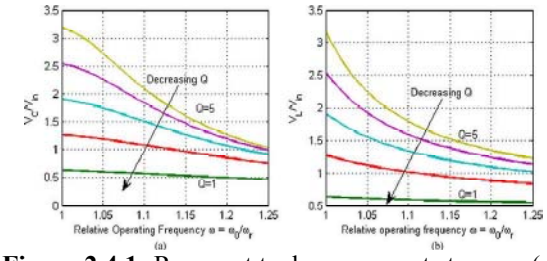


Figure 2.4.1: Resonant tank component stresses. (a) Capacitor. (b) Inductor.

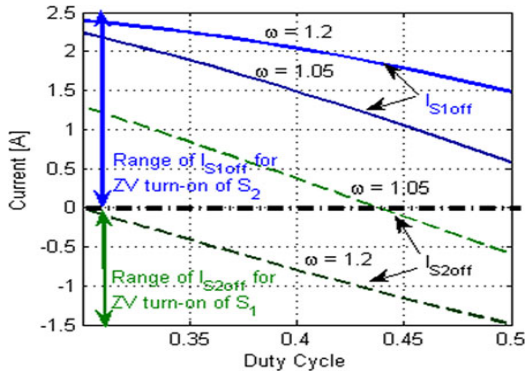


Figure 2.4.2: Turn-off currents at full load with input voltage variation

IS2 off at minimum duty cycle. Therefore, a compromise must be made to reduce circulating current of the tank and auxiliary network.

2.3.3. Auxiliary Inductor and Snubber Capacitors

The key equation governing the achievement of ZVS is given by (20), which states that in a given charge interval, the charge held by the snubber capacitors must be less than the charge removed by the auxiliary inductor Qa and resonant tank Qr. For some operating points, the resonant current aids in discharging the snubber capacitors, while at other operating points, it works against the auxiliary network.

$$C_{sb}V_{in,max} \leq \int_{T_{ch}} i_a dt + \int_{T_{ch}} i_r dt.$$

To solve the charge inequality, the auxiliary and resonant currents must be integrated during the respective capacitor charge periods. While the charge itself is independent of Vin, the contribution of the resonant current is dependent on the duty cycle of the drive train, which is a function of the input voltage. The influence of the turn-off currents is demonstrated in the figures by the reduced charge time experienced during Tch2 for a given inductor/capacitor combination.

To achieve zero-voltage turn-off, the rate of rise of the drain, Source voltage should be at least twice as long as the fall time of the current in the switch. Thus, Figure provides the minimum component values for true ZVS. Since Tch1 is greater than Tch2 for a given configuration, it follows that both switches will achieve lossless transitions at both turn-on and turn-off. Reduction of the turn-off current of S1 occurs with reduction of input voltage or load. Thus, Tch2 will increase from the full-load, high-line level, thereby further reducing the turn-off loss of the switch. Conversely, increased duty cycle will cause the resonant current to work with the auxiliary current during Tch1. This will reduce the charge time from the high-line value.

In addition to achieving ZVS, conduction loss, size, and cost are important factors to consider. Therefore, the auxiliary inductor and snubber capacitor selection should strike a compromise of these added issues. While lower inductance values reduce the size of the magnetic component, they increase the required snubber capacitance, and increase conduction loss. The latter requires switches with higher current ratings, and potentially large heat sinks, thereby negating any savings. Larger auxiliary inductors reduce conduction loss and snubber capacitor requirements at the expense of magnetic component size.

3. Proposed System Design Objective

The objective of the project is to simulate and implement the Series-Resonant APWM Converter.In this project,the high-frequency operation is necessary to reduce the size of

reactive components. Furthermore, soft switching, either zero voltage switching (ZVS) or zero current switching (ZCS), is required for efficient operation to reduce or eliminate heat sink requirements. Resonant converters have been well documented 0 to meet both of these requirements of the different resonant tank structures; the series-resonant converter is the simplest structure that has inherent protection against transformer saturation. It promotes high efficiency through ZVS of the primary switching devices, ZCS of its rectifiers, and load-dependent current.

3.1 Proposed Circuit

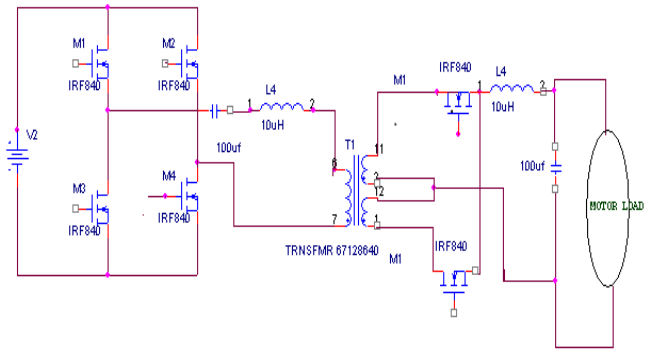


Figure 2.5: Diagram of Proposed Circuit

3.1.1. Operation of Proposed circuit

The full bridge inverter consists of four MOSFETs and four diodes. In positive half cycle, when M1and M4 conducts, load voltage is Vs and when M2 and M3 conduct load voltage is –Vs. Frequency of output voltage can be controlled by varying the periodic time T. MOSFETs M1, M4 or M2, M3 are in series across the source during the inverter operation it should be ensured that two MOSFETs in the same branch, such as M1, M4. For a resistive load, two MOSFETs would suffice, because load current i_0 and load voltage v_0 would always be in phase with each other. This, however, is not the case when the load is other than resistive. For such types of loads, current i_0 will be in phase with voltage v_0 and diodes connected in antiparallel with MOSFETs will allow the current to flow when the main MOSFETs are turned off. As the energy is fed back to the source when these diodes conduct, these are called feedback diodes.

3.1.2. Gate Pulse

F= 10 KHz
T= 1/10= 0.1ms
T=100µs

3.1.3. Duty Cycle

Duty Cycle = 50%
T_{ON} = 0.5*100
T_{ON} =50 µs
T_{OFF} = 0.5*100
T_{OFF} = 50 µs

3.1.4Delay Calculation

Machine Cycle = 4/f0
Delay Time = 3[1+No.of machine cycles]*Machine cycle

3.2. Efficiency Calculation

Vo= 15V
R= 10Ω
I=Vo/R
I=15/10
I=1.5A

POWER P= VI watts
= 15*1.5
P = 22.5 Watts
Transformer Loss = 0.25W

Conduction Loss = 2δVdsI
= 2*0.5*1*1.5
ώc = 1.5W
Assume R=0.1 Ω
Inductor Loss = I^2R
=1.5^2*0.1
ώl = 0.225W

Efficiency ή = Po/Po+ώc+ώt+ώl
= 22.5/22.5+0.25+1.5+.225
ή = 91%

3.2 Relation between Φ and F

E = K Φ f

Here E, K are constants. So, Φ = E/Kf
Φ α 1/f

So flux is inversely proportional to frequency.

The converter designed in the previous section has been simulated in the spice simulator SIMetrix. The figures have been annotated to show that both switches achieve zero-voltage turn-off and turn-on. As discussed in the previous section, the two charge intervals at low line are almost the same due to the nearly symmetric ac component of the drive voltage at this operating point. At high line, Tch2 is slightly greater than four times the fall time of the switch, thus ensuring zero-voltage turn-off of S1 even at this extreme operating point.

A comparison of the proposed design with the original at 1MHz is presented in Table II. The resonant inductor is formed by the transformer leakage, and therefore fixed. The original design operated further from the resonant frequency, and had a larger auxiliary inductor. The former theoretically helps achieve ZVS and the latter reduces circulating current. By operating close to the resonant frequency, circulating current associated with the resonant tank is minimized with minimal impact on the energy required by the auxiliary network. Moreover, zero-voltage

transitions are guaranteed at any operating point at both turn-on and turn-off.

3.3. Experimental Results

An experimental prototype of a modified series-resonant APWM converter has been built to meet the specifications of Table I. The components used are given in Table III. In selecting the external snubber capacitance, the contribution of the MOSFETs should be known. MOSFET output capacitance Coss is the sum of the drain. Gate and drain Source capacitance of the device. This behavior is beneficial for eliminating turn-off loss since the effective capacitance is larger at the turn-off instant and reduces as the voltage rises.

Source voltage (Vds, spec), and Vds, off is the voltage across the device in the user fs application

$$C_{\text{oss,ave}} = 2C_{\text{oss,spec}}\sqrt{\frac{V_{\text{ds,spec}}}{V_{\text{ds,off}}}}.$$

For the FDMS86104 devices used in this study, Coss,ave is calculated to be 346 pF per device at 53V, and 383 pF at 43V. At low input voltage, the duty cycle is ideally saturated at 50% and the charge times are identical.

The small difference between the measured charge times can be attributed to the duty cycle being slightly lower than ideal with uneven dead time between the switches. Thus, the turn-off current of the switches is slightly asymmetric. At that instant of time, the drain Source voltage is 1.72V, which means that while in the linear region, the voltage across S2 was only able to rise to 3.25% of its final value. This shows that the turn-off losses of S2 are nearly lossless. While Vgs1 is not shown, extrapolating the results of S2 indicates that the voltage across S1 is likely 5% of its final value by the time the gate. Source voltage falls to the threshold voltage. This provides a substantial reduction in switching loss at this worst case operating point.

The absence of resonant current extends the fall times of the drain. Source voltage compared to the respective full-load cases of significance is the fact that at any input voltage or load condition, the rise and fall times are always greater than four times the fall time of the switch current. Therefore, ZVS is achieved at every operating point.

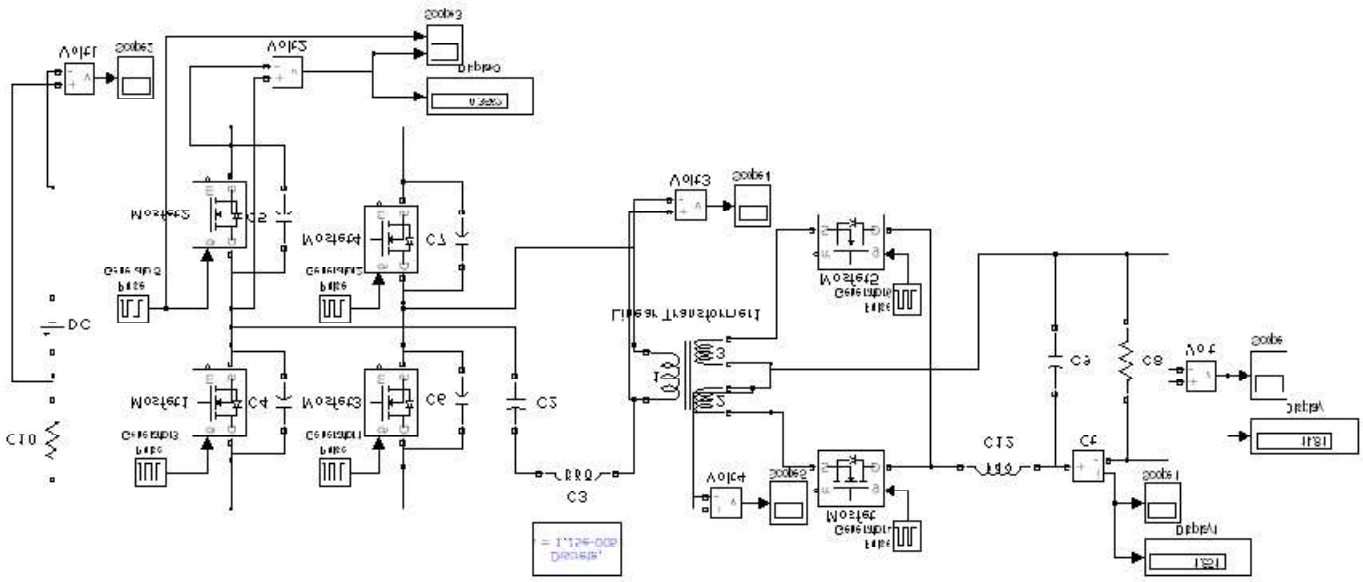


Figure 3.3.1: Simulation Circuit of proposed converter

The full bridge inverter consists of four MOSFETs and four diodes. In positive half cycle, when M1and M4 conducts, load voltage is Vs and when M2 and M3 conduct load voltage is –Vs. Frequency of output voltage can be controlled by varying the periodic time T.

MOSFETs M1, M4 or M2, M3 are in series across the source during the inverter operation it should be ensured that two MOSFETs in the same branch, such as M1, M4. For a resistive load, two MOSFETs would suffice, because load current i_0 and load voltage $v_0$would always be in phase with each other. This, however, is not the case when the load is other than resistive. For such types of loads, current i_0 will be in phase with voltage v_0 and diodes connected in antiparallel with MOSFETs will allow the current to flow when the main MOSFETs are turned off. As the energy is fed back to the source when these diodes conduct, these are called feedback diodes. By using MATLAB Simulink the input and output waveforms are described below.

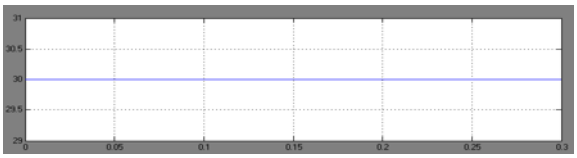


Figure 3.3.2: Input Voltage

The above waveform is the input voltage waveform. Here DC input voltage of 30V is given to the Inverter.

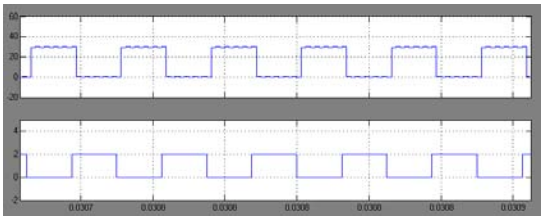


Figure 3.3.3: Switching Pulse and Vds Voltage

The above waveform describes the switching pulses and Vds voltage of the inverter in the input side. The gate pulse given to the switch is 100µs and a duty cycle of 50 µs for ON and OFF time

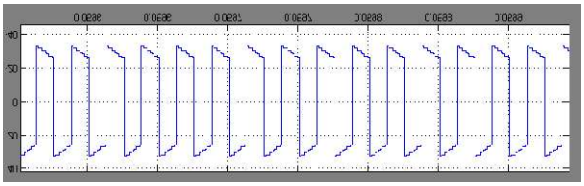


Figure 3.3.4: Transformer primary Voltage

The above waveform represents transformer primary voltage in the primary side.

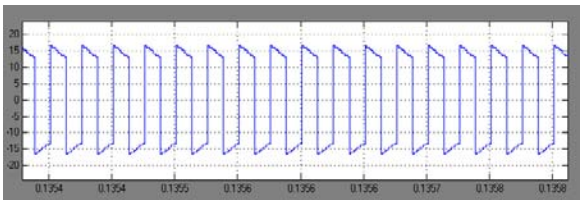


Figure 3.3.5: Transformer secondary Voltage

The above waveform represents transformer secondary voltage in the secondary side.

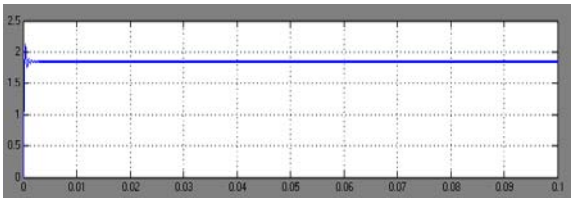


Figure 3.3.6: Output current

The Output Current $Io = \frac{Vo}{R}$ shows that the output current rises and attain a maximum value of up to 1.8A which is 1.5A greater than the conventional method.

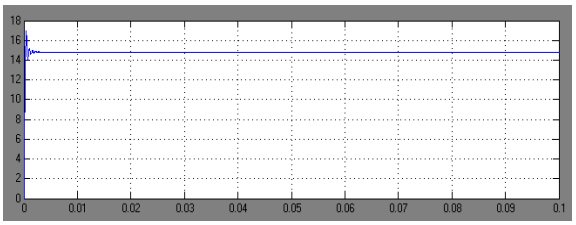


Figure 3.3.7: Output voltage

The above waveform shows the output voltage of 15V obtained from the full bridge inverter. The inverter operation done here is same as buck converter operation. In buck converter the output voltage is half of the amount of input voltage. So from 30V of input we obtained the actual output voltage.

3.4 Proposed Circuit with Motor Load

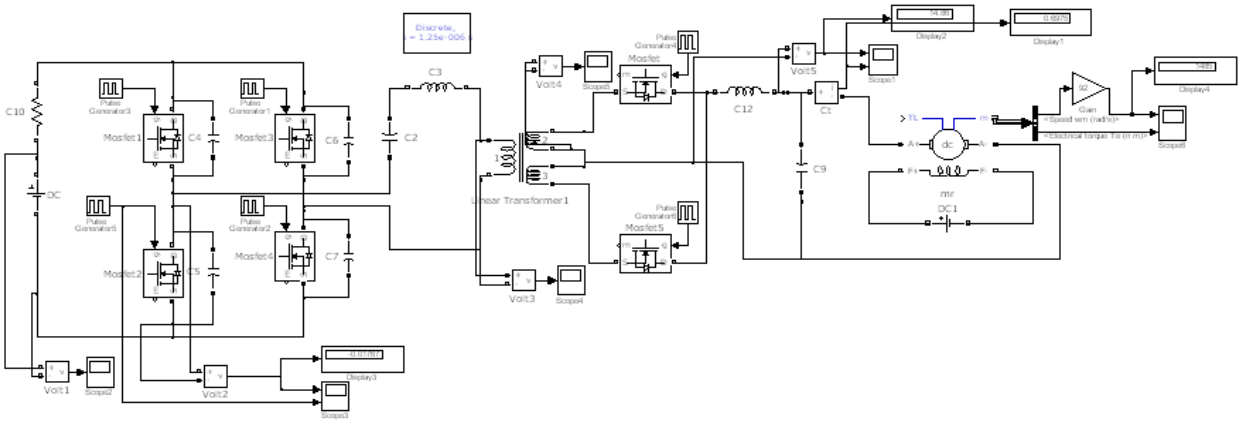


Figure 3.4.1: Simulation Circuit of proposed converter with motor load

The full bridge inverter consists of four MOSFETs and four diodes. In positive half cycle, when M1and M4 conducts, load voltage is Vs and when M2 and M3 conduct load voltage is –Vs. Frequency of output voltage can be controlled by varying the periodic time T.MOSFETs M1, M4 or M2, M3 are in series across the source during the inverter operation it should be ensured that two MOSFETs in the same branch, such as M1, M4. For a resistive load, two MOSFETs would suffice, because load current i_0 and load voltage v_0 would always be in phase with each other.

For Hardware implementation a motor either DC or SERVO load has to be fixed for real time applications. We can measure the speed in rpm and torque output in N-m.

The Simulation output is given below.

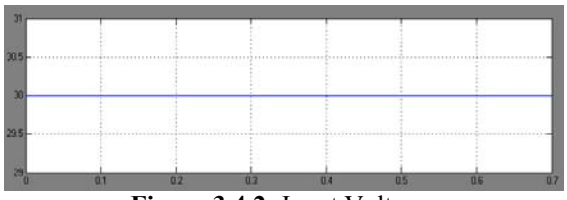


Figure 3.4.2: Input Voltage

The above waveform is the input voltage waveform. Here DC input voltage of 30V is given to the Inverter.

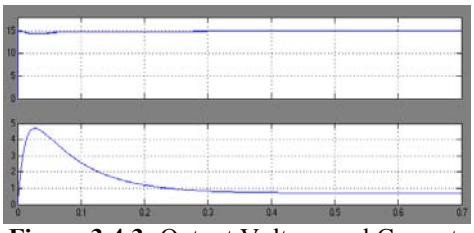


Figure 3.4.3: Output Voltage and Current

The above waveform shows the output voltage of 15V obtained from the full bridge inverter. The inverter operation done here is same as buck converter operation. In buck converter the output voltage is half of the amount of input voltage. So from 30V of input we obtained the actual output voltage.

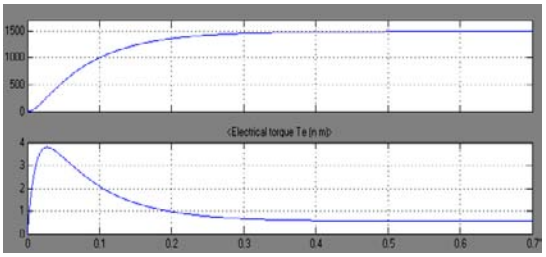


Figure 3.4.4: DC Motor speed and torque output

The DC motor speed is measured in rpm and runs at a speed of 1500 rpm at a constant speed. The Torque output is measured and it rises from 0 to 4N-m and decreases to steady state below one N-m.

3.5 Proposed Circuit with Disturbance

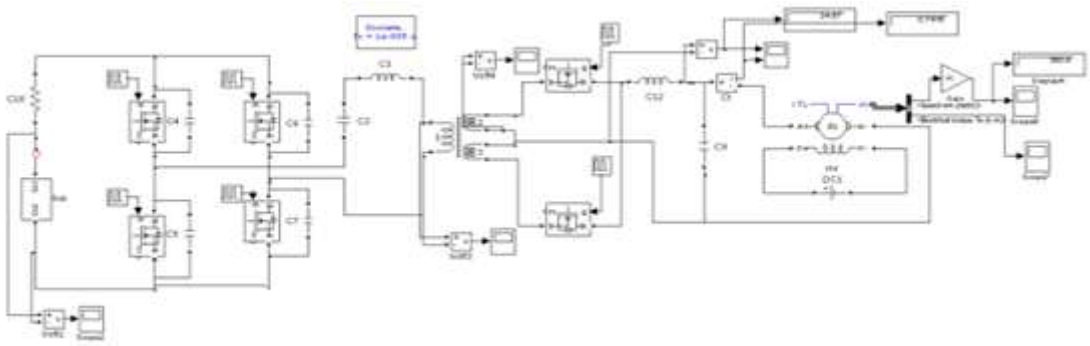


Figure 3.5.1: Simulation Circuit of proposed full bridge converter with disturbance

If a disturbance arises in the input or output side, the output results totally changes and a steady state error is created. To avoid the steady state error the closed loop control of PI or PID controller is preferred.

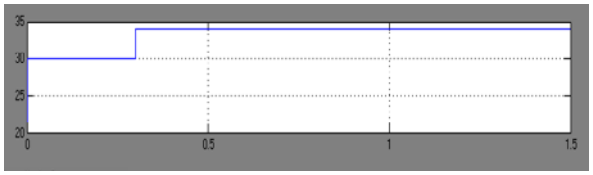


Figure 3.5.2: Input Voltage

The disturbance created in the circuit changes the input voltage from 0 to 30V and then to 35 V. So a steady state error is created in the input voltage.

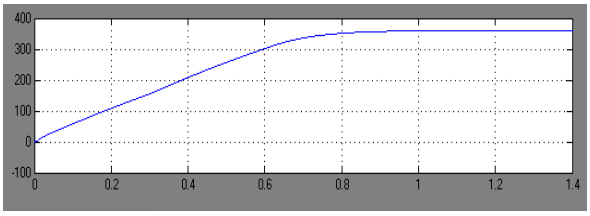


Figure 3.5.3: Motor Speed

The disturbance created in the circuit changes the motor speed from 0 to 350 rpm and then to oscillation level. By steady state error, the motor speed reduces to a lower level below the actual level.

3.6 Proposed Circuit with Closed Loop Control

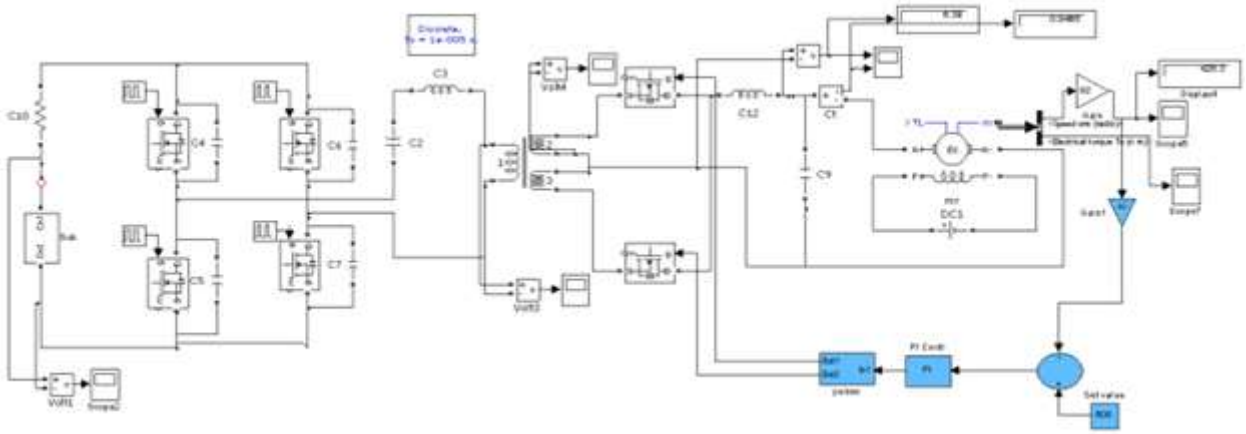


Figure 3.6.1: Simulation Circuit of Closed loop control of proposed converter

The Closed loop control of proposed converter employs a PI controller to avoid a steady state error. The Time response of a system is measured in the closed loop control and the Output voltage regained its actual value and DC motor also runs at original speed and torque.

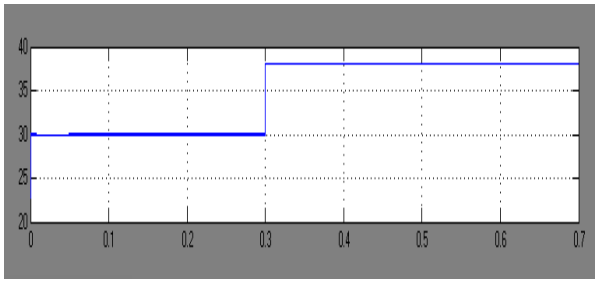


Figure 3.6.2: Input Voltage

By using PI controller the input voltage is controlled and a constant input value is given to the inverter.

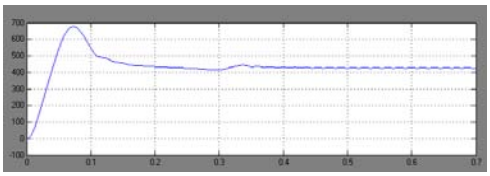


Fig: 3.6.3: Motor Speed

By closed loop control method using PI controller the steady state error is reduced and the motor runs at a constant speed of rpm throughout the operation.

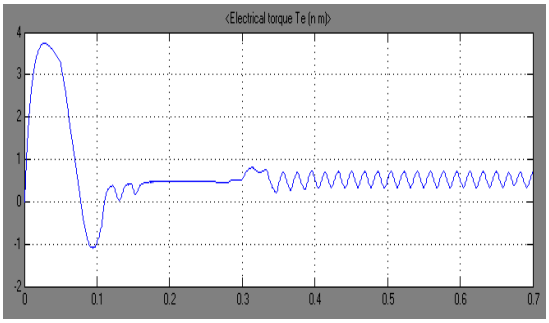


Figure 3.6.4: Torque

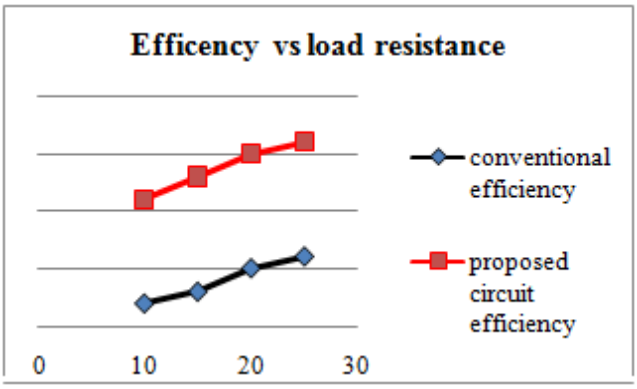
The above waveform clearly shows that the motor torque retain the original position after using closed loop control with PI controller by reducing the steady state error. The Motor runs at a constant speed and torque of 91% efficiency which is 9% higher than the conventional method.

3.7 Efficiency Comparison

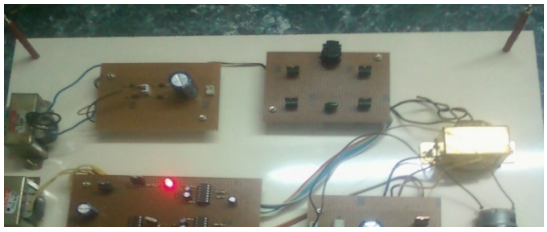
By varying the load resistance, the conventional and proposed circuit efficiency is compared. The Simulation results have 91% efficiency which is 9% higher than the conventional method. The efficiency comparison is given below.

Table 3.7: Efficiency comparison

Load resistance (Ro) ohm	*Conventional Efficiency %*	*Proposed circui Efficiency %*
10	82	91
15	83	93
20	85	95
25	86	96



4. Hardware Kit Diagram



The hardware circuit consists of Power Circuit and Control Circuit. The Power supply circuit has a step-down transformer (230/15) V is used to give input supply to the power circuit. The 15V AC input is rectified into 15V pulsating DC with the help of full bridge rectifier circuit. The ripples in the pulsating DC are removed and pure DC is obtained by using a capacitor filter. The positive terminal of the capacitor is connected to the input pin of the 7812 regulator for voltage regulation. An output voltage of 12V obtained from the output pin of 7812 is fed as the supply to the pulse amplifier.

An output voltage of 5V obtained from the output pin of 7805 is fed as the supply to the micro controller. From the same output pin of the 7805, a LED is connected in series with the resistor to indicate that the power is ON. The hardware is implemented using the PIC- Microcontroller "PIC 16F84A". The PIC16F84A can be operated in selectable crystal oscillator. It is used to produce the gate pulse to the switch. The gate pulse produced here is 5V, but we need minimum 10V to trigger the MOSFET switch. So we are going for a Driver Amplifier circuit. By means of this Driver unit 5V is amplified to 10V to trigger the MOSFET. Then the DC is converted to AC with high frequency.

So the size of the reactive components is reduced. Next the AC supply is step down to 15V and rectified to DC and fed to the load. The power circuit consists of four MOSFETs and four diodes. In positive half cycle, when M1and M4 conducts, load voltage is Vs and when M2 and M3 conduct load voltage is –Vs. Frequency of output voltage can be controlled by varying the periodic time T.

MOSFETs M1, M4 or M2, M3 are in series across the source during the inverter operation it should be ensured that two MOSFETs in the same branch, such as M1, M4. For a resistive load, two MOSFETs would suffice, because load current i_0 and load voltage v_0 would always be in phase with each other. This, however, is not the case when the load is other than resistive. For such types of loads, current i_0 will be in phase with voltage v_0 and diodes connected in antiparallel with MOSFETs will allow to flow when the main MOSFETs are turned off. As the energy is fed back to the source when these diodes current conduct, these are called feedback diodes.

4.1 Hardware Output Voltage across resistor load

Figure 4.11.1: Hardware Output voltage across resistor load

The above waveform shows the output voltage of 15.5V obtained from the hardware circuit across resistor load. The inverter operation done here is same as buck converter operation. In buck converter the output voltage is half of the amount of input voltage. So from 30V of input we obtained the output voltage of 15.5V.

4.1.1 Hardware Motor Output

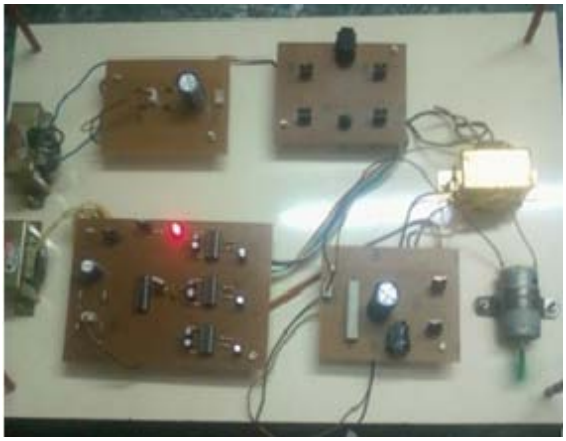


Figure 4.1.1 Hardware Motor Output

The above diagram shows the motor load output of hardware kit. For a real time application a PMDC motor of 24V, 0.5A is attached parallel to the R load. The motor is running at a speed of 1500 rpm at its output side.

4.12 Applications

1) Speed Control of DC Motor
2) Speed Control of SERVO Motor
3) Battery Charging
4) X-ray Unit
5) High speed digital device applications.

5. Conclusion

The modified topology has been analyzed and a prototype was built. Not only did it overcome the limitations of the original topology, but also the concept is simple and not many extra components are required. It offers Zero voltage switching over an input voltage range of 30 to 80 volts. Based on experimental results from the prototypes, its overall efficiency is 9% higher than that of the original. Due to compensating feature of the auxiliary network providing a lower voltage stress across the resonant inductor, with a diode rectifier in the output stage, the power loss is quite significant. The use of MOSFETs in synchronous rectification can reduce this power loss. For current fed topologies, the gating signals must be developed from the secondary currents of the main transformer and not their voltages, for proper rectifier operation.

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Author Profile

Devaraj .N Received the B.E, Degree. in Electrical and Electronics Engineering From Meenakshi Academy of Higher Education and Research (MAHER) Chennai-78, and currently doing M. Tech. degree in Power Electronics and Drives from Bharath Institute of Science and Technology, Chennai, affiliated to Bharath University, Chennai-73, India

K. S. S. Prasad Received the B.E Degree in Electrical and Electronics Engineering, from Andhra University and M.Tech degree in Embedded Systems. From Bharath Institute of Science and Technology, Chennai, affiliated to Bharath University, Chennai-73. He now works as Assistant Professor in Bharath Institute of Science and Technology, Chennai-73, India.