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Three Phase Dual Output Inverters for Photo Voltaice System with Three Switch Legs

Sakthivel K[1], B. Vaidianathan[2]

[1]PG Scholar, Bharath University, Chennai, India

[2]Assistant Professor[2], Bharath University, Chennai, India

Abstract: ***In this paper, three reduced switch count topologies are introduced for independently supplying two three-phase ac loads with one inverter for solar based power generation is proposed. Using a new three-switch leg structure recently introduced and implemented in three-phase converters. The proposed nine-switch topologies are introduced; two modes of equal frequency and different frequency operation each of its own distinctive characteristics are considered for them and their pulse width modulation schemes are elaborated. Comprehensive analyses of power loss profile and output waveform properties are conducted via simulation for the proposed inverters, and the results are compared with full-bridge and half-bridge inverters. To assess the performance of the proposed inverter topologies, working prototypes are built, and the experimental results are provided.***

Keywords : photovoltaic system, three phase supply, dc to dc boost converter, xor gate, two ac load output.

1. Introduction

Inverter is an electrical power converter that changes direct current (DC) to alternating current (AC).[1] The input voltage, output voltage, and frequency are dependent on design [1]. Static inverters do not use moving parts in the conversion process. Some applications for inverters include converting high-voltage direct current electric utility line power to AC, and deriving AC from DC power sources such as batteries [1-8]. The word 'inverter' in the context of power-electronics denotes a class of power [4] conversion (or power conditioning) circuits that operates from a dc voltage source or a dc current source and converts it into ac voltage or current.[5]

The 'inverter' does reverse of what ac-to-dc 'converter' does (refer to ac to dc converters) [2]. Even though input to an inverter circuit is a dc source, it is not uncommon to have this dc derived from an ac source such as utility ac supply. Thus, for example, the primary source of input power may be utility ac voltage supply that is 'converted' to dc by an ac to dc converter[2] and then 'inverted' back to ac using an inverter.[5] Here, the final ac output may be of a different frequency and magnitude than the input ac of the utility.

2. Scope

To use three phase supply to get two ac loads, to reduce the switching devices on converter and Overall cost of the system will be low compared with conventional method.

3. Proposed Methodology

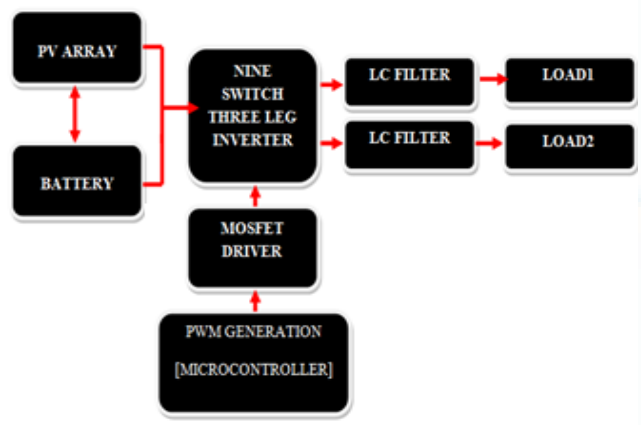

Figure 1: block diagram

The simplest dc voltage source for a VSI [3] may be a battery bank, which may consist of several cells in series-parallel combination. Solar photovoltaic cells can be another dc voltage source. An ac voltage supply, after rectification into dc will also qualify as a dc voltage source. A voltage source is called stiff, if the source voltage magnitude does not depend on load connected to it. All voltage source inverters assume stiff voltage supply at the input [3].

Some examples where voltage source inverters are used are: uninterruptible power supply (UPS) units, adjustable speed drives (ASD) for ac motors, electronic frequency changer circuits etc. Most of us are also familiar with commercially available inverter units used in homes and offices to power some essential ac loads in case the utility ac supply [6] gets interrupted. In such inverter units, battery supply is used as the input dc voltage source and the inverter circuit converts the dc into ac voltage of desired frequency. The achievable magnitude of ac voltage is limited by the magnitude of input (dc bus) voltage. In ordinary household inverters the battery voltage may be just 12 volts and the inverter circuit may be capable of supplying ac voltage [8] of around 10 volts (rms)

only. In such cases the inverter output voltage is stepped up using a transformer to meet the load requirement of, say, 230 volts.

3.1 A push-pull active amplifier circuit and a push pull switched mode circuit

show two schematic circuits, using transistor-switches, for generation of ac voltage from dc input supply. In both the circuits, the transistors work in common emitter configuration and are interconnected in push-pull manner. In order to have a single control signal for the transistor switches, one transistor is of n-p-n type and the other of p-n-p type [1] and their emitters and bases are shorted as shown in the figures. Both circuits require a symmetrical bipolar dc supply. Collector of n-p-n transistor is connected to positive dc supply (+E) and that of p-n-p transistor is connected to negative dc supply of same magnitude (-E). Load, which has been assumed resistive, is connected between the emitter shorting point and the power supply ground.

The transistors work in active (amplifier) mode and a sinusoidal control voltage of desired frequency is applied between the base and emitter points. When applied base signal is positive, the p-n-p transistor is reverse biased and the n-p-n transistor conducts the load current. Similarly for negative base voltage the p-n-p transistor conducts [1] while n-p-n transistor [7] remains reverse biased. A suitable resistor in series with the base signal will limit the base current and keep it sinusoidal provided the applied (sinusoidal) base signal magnitude is much higher than the base to emitter conduction-voltage drop. Under the assumption of constant gain (h_{fe}) of the transistor over its working range, the load current can be seen to follow the applied base signal. A typical load voltage (in blue color) and base signal (green color) waveforms.[5] This particular figure also shows the switch power loss for n-p-n transistor (in brown color). The other transistor will also be dissipating identical power during its conduction. The quantities are in per unit magnitudes where the base values are input supply voltage (E) and the load resistance (R). Accordingly the base magnitudes of current and power are E/R and E^2/R respectively. As can be seen, the power loss in switches is a considerable portion of circuit's input power and hence such circuits are unacceptable for large output power applications [8].

The conducting switch remains fully on having negligible on-state voltage drop and the non-conducting switch remains fully off allowing no leakage current through it. The load voltage waveform output by switched-mode circuit is rectangular with magnitude +E when the n-p-n transistor [1] is on and –E when p-n-p transistor is on. Shows one such waveform (in ink color). The on and off durations of the two transistors are controlled so that (i) the resulting rectangular waveform has no dc component (ii) has a fundamental (sinusoidal) component of desired frequency and magnitude and (iii) the frequencies of unwanted harmonic voltages are much higher than that of the fundamental component. The fundamental sine wave, shown in blue color, is identical to the sinusoidal output voltage.

Both amplifier mode and switched mode circuits are capable of producing ac voltages [8] of controllable magnitude and frequency, however, the amplifier circuit is not acceptable in power-electronic applications due to high switch power loss. On the other hand, the switched mode circuit generates significant amount of unwanted harmonic voltages along with the desired fundamental frequency voltage. As will be shown in some later lessons, the frequency spectrum of these unwanted harmonics can be shifted towards high frequency by adopting proper switching pattern. These high frequency voltage harmonics [3] can easily be blocked using small size filter and the resulting quality of load voltage can be made acceptable.

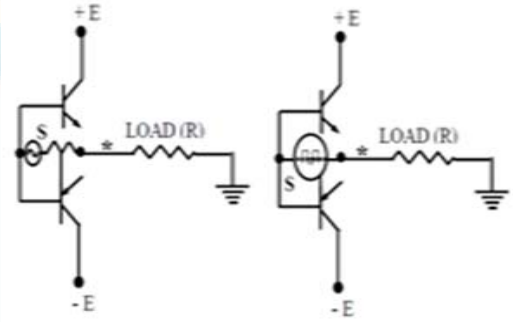

Figure 1: (a) A push pull active amplifier Circuit (b) A push pull switched mode Circuit

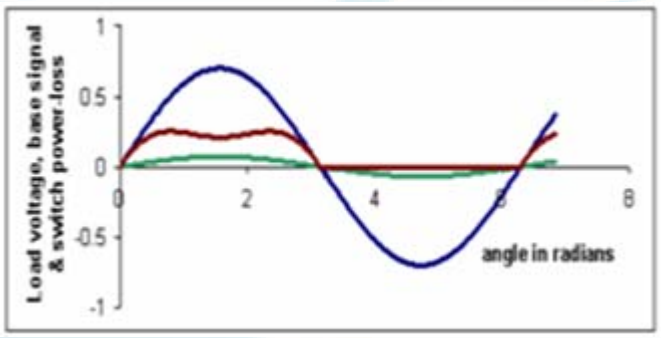

Figure 2: (a) Switch in amplifier mode operation

3.2 Half-Bridge VSI

The power topology of a half-bridge VSI [1], consists of two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage [3] (Vi)/2. Because the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors (C+ and C-) is required. It is clear that both switches S+ and S- cannot be ON simultaneously because a short circuit across the dc link voltage source Vi would be produced. There are two defined (states 1 and 2) and one undefined (state 3) switch state as In order to avoid the short circuit across the dc bus and the undefined ac output voltage [2] condition, the modulating technique should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.

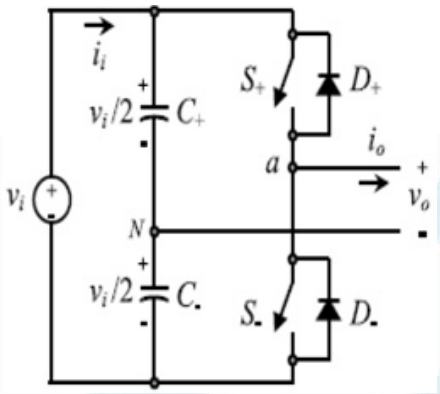

Figure 3: Single-phase half-bridge VSI

3.3 Full-Bridge VSI

This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load. As expected, both switches S1+ and S1- (or S2+ and S2-) cannot be on simultaneously because a short circuit across the dc link voltage source [5] Vi would be produced. There are four defined (states 1, 2, 3, and 4) and one undefined (state 5) switch states.

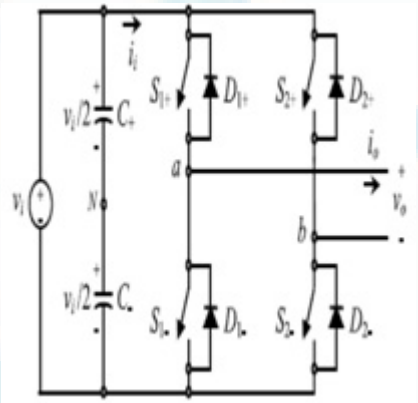

Figure 4: Single phase full bridge vsi

The undefined condition should be avoided so as to be always capable of defining the ac output voltage. It can be observed that the ac output voltage can take values up to the dc link value Vi, which is twice that obtained with half-bridge VSI topologies. Several modulating techniques [1] have been developed that are applicable to full-bridge VSIs. Among them are the PWM (bipolar and unipolar) techniques.

3.4 Three Phase Voltage Source Inverters

Single-phase VSIs cover low-range power applications and three-phase VSIs cover the medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g., ASDs, UPSs, FACTS, VAR compensators), arbitrary voltages are also required in some emerging applications (e.g., active filters, voltage compensators) [6].

The standard three-phase VSI topology is shown and the eight valid switch states. As in single-phase VSIs, the switches of any leg of the inverter (S1 and S4, S3 and S6, or S5 and S2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, [2] and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity. Of the eight valid states, two of them produce zero ac line voltages [5]. In this case, the ac line currents freewheel through either the upper or lower components. The remaining states produce non-zero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus the resulting ac output line voltages consist of discrete values of voltages that are Vi, 0, and -Vi for the topology. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states.

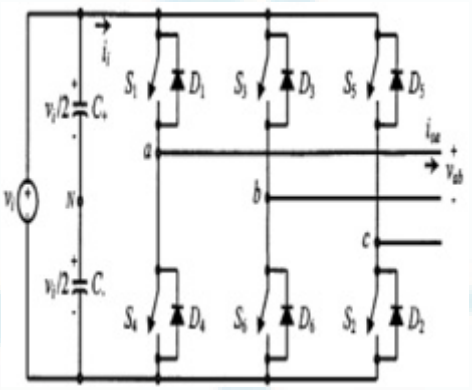

Figure 5: Three-phase VSI topology

3.5 Dual output inverter

A two-output series resonant inverter fulfils the requirements of a multiple burner arrangement in induction cooking appliances. It uses a fixed frequency control technique for the control of output power and ensures ZVS operation with independent and simultaneous control of the two loads. It has many advantages over single output inverters such as less component count, sharing of converter components, [1] higher utilization of power electronic equipment, cost-effectiveness as well as maximization of power at any one of the loads. Considering two full-bridge inverters supplying two different loads and their switching sequence of various switches, we can infer that two legs of these inverters can be merged into a common leg and considered as one resulting in a three-legged topology of a single inverter supplying two different loads.[4] This inverter topology as shown in figure 5 comprises of two independent legs and one common leg achieving saving in the number of switches from the two inverter configuration.

Due to the various disadvantages of variable frequency output power control techniques such as electromagnetic noise spectrum and acoustic noise, it is generally preferred to use fixed-frequency control to reduce noise and electromagnetic interference. In addition to this it is also

desired to ensure ZVS for minimum switching losses. It takes place when the switching frequency [4] is slightly above the resonant frequency of the inverter [1]. If switching frequency is taken much larger than the resonant frequency, it results in lower efficiency due to circulating currents and low power factor of load. The following control techniques can be explained by using a quasi-square wave of output voltage shown in fig. having four control variables, namely, the control angles α+ ,α- and β and the switching period T. As we are maintaining constant frequency, the control parameter T remains constant.

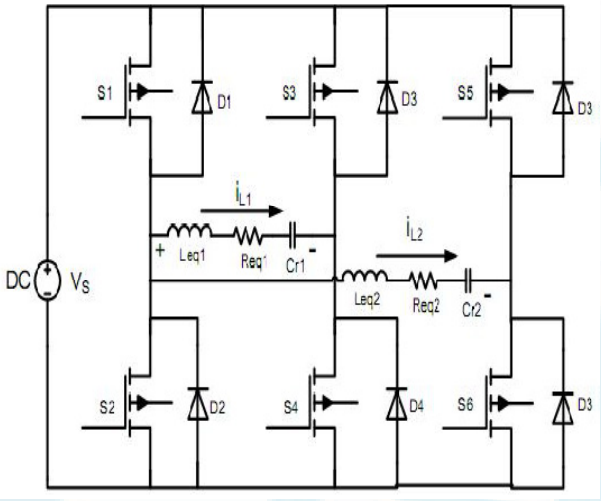

Figure 6: Two output inverter configuration

3.6 Phase shift control method

The phase shift control method, also known as clamped-mode control method employed generally for full bridge inverters. In this control technique, symmetrical voltage cancellation is achieved in which the switching pulse sequences are shifted by a certain phase with respect to one another keeping the pulse width constant. [8] The control parameters α+ = α- are varied by equal amounts and β = 180: is kept constant in the quasi-square output voltage wave by providing the phase shift in switching pulses.

3.7 Asymmetrical Voltage Cancellation method

It is a generalized power control technique applied to series resonant inverters employed for induction heating applications. In this technique, the pulse width or duty cycle are unequal and varied accordingly to control the output voltage [1] or power in an inverter. The control parameters α+ and α- are kept constant and β is varied in the quasi-square output voltage wave by providing the duty cycle control.

3.8 Simulation Methodology

Figure 7 shows the structure of the proposed nine-switch inverter. It consists of two three-switch legs and two single-phase loads connected to the joints between the switches. The dual-leg structure can be considered as two full-bridge inverters which share a row of switches (the middle switches of the proposed structure). Consequently, the proposed configuration reduces the number of switches by 25%. The two output voltages can be expressed as $Vox = MxVg\text{Sin}(\omega xt + \phi x)$_where x denotes upper or lower output_ similar to single-phase full bridge inverter except that some constraints are imposed on the modulation indices, frequencies, ω, and phase difference, ϕ of the output references depending on the subsequently defined equal frequency (EF) and different frequency (DF) operation modes. Compared to two-switch leg which creates four possible switching states of which two are acceptable, three-switch leg can create eight states; to avoid dc bus short-circuit and floating of the loads, only the three switching [2] states of Table I are acceptable. Totally, the inverter has nine switching states of which the OFF and ON switch states are, respectively, represented by dotted and solid lines. Opposite and negative current paths of the upper and lower loads are also indicated in the figure. As it can be seen in Fig.[6] when the switches of the same row are OFF both outputs are in zero state (a, e, and i), when the upper or lower switch rows are ON, the corresponding output is in zero state (b, d, f, and h) and the other is in active state and finally,

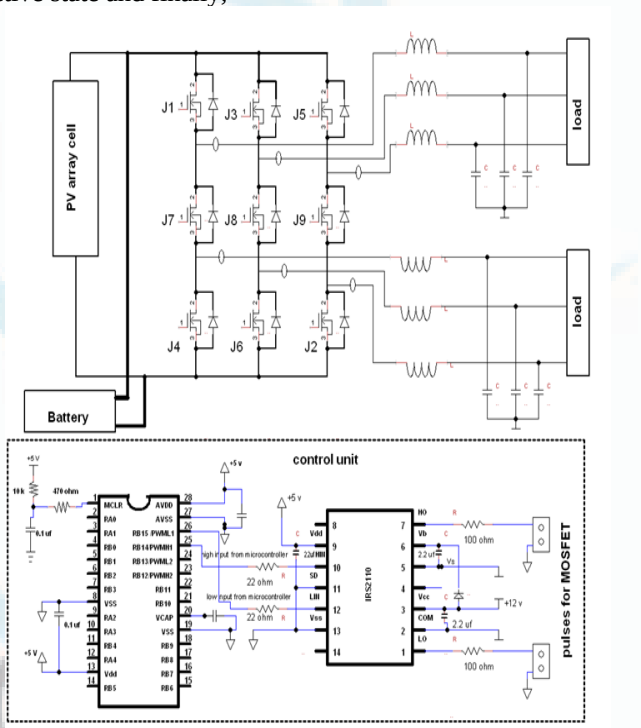

Figure 7: Simultation Circit diagram

when the opposite switches of the two legs are OFF, both outputs [2] are in active state (c and g). Using these states, two modes of operation are definable considering frequency/amplitude independency of the output voltages as follows.

3.9 Different Frequency Mode of Operation

In this mode, the two ac outputs are independent from each other regarding both frequency and amplitude. From the formerly obtained switching states, those by which two loads are simultaneously connected to the dc supply should never be used otherwise; outputs will lose their frequency independency. In other words, the switching states applied

to the inverter legs should be either S1–S2 when the upper output is active whereas the lower output voltage is zero or S2–S3. When the lower output is active where as the upper output voltage is zero. As in Three-phase type, this criterion is easily fulfilled by sharing the total modulation index between the outputs via shifting their corresponding references in different directions in the space occupied by carrier signal (modulation space).

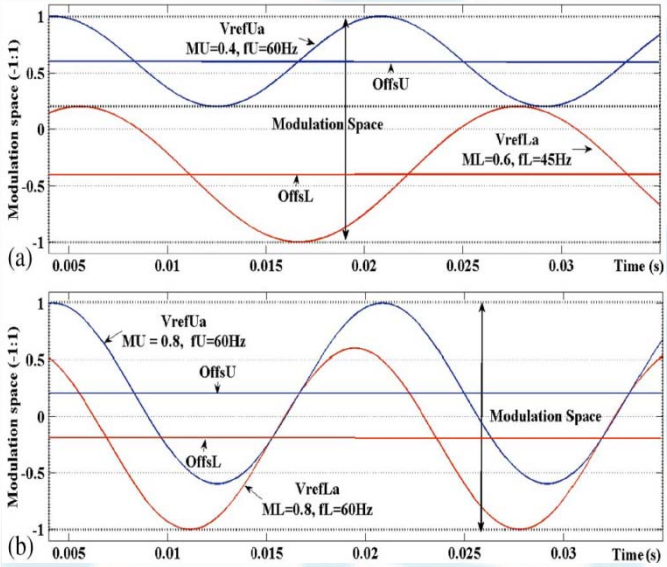

Figure 8: Modulation space division. (a) DF mode. (b) EF mode.

Hence, the principal condition of working in this mode is that the sum of modulation indices must be less than one. As shown in Fig., shifting the references in the modulation space is accomplished by adding appropriate offset values to them. To fully utilize dc bus voltage, the offset values are determined considering each output required maximum modulation index via defining α as distribution coefficient in

$$\alpha = |VrefU| \; |VrefU| + |VrefL| \; 0 \le \alpha \le 1 \quad (1)$$

Where *VrefU* and *VrefL* are the upper and lower reference signals, respectively. Obtaining the distribution coefficient, the offset values for upper and lower outputs would be $1 - \alpha$ and $-\alpha$, respectively. Gate signals of the upper and lower switches are generated by comparing the modulating signals with the carrier signal. Middle switch gate signals are logical XOR of the upper and lower gate signals of the same leg [1]

3.10 Equal Frequency Mode of Operation

If the frequencies of the output voltages are equal, the inverter can be used in EF mode in which, depending on the phase difference between the references, it is possible for both outputs to have modulation indices up to one. Despite DF operation in which c and g switching states of Fig could not be used; all the switching states are possible in this mode since frequency independency of the outputs is forfeited. It is worth noticing that when the outputs are in phase and their modulation index is the same, the middle switches will always be ON, (a, c, g, and i switching states of Fig. and the inverter works exactly similar to a full-bridge inverter [1] with two parallel loads connected to it. In case the references are in phase, the sum of modulation indices can reach up to two. Whether the references are in phase or not, the condition of (2) should be satisfied (upper output modulating waveform should always be higher than the lower output modulating waveform) and in order to avoid modulating wave interference, appropriate offsets should be added to the references; for the widest range of modulation space utilization (3) might be used

$$1 + MU\,(\sin(\omega t + \delta) - 1) \ge ML\,(\sin(\omega t) + 1) - 1 \quad (2) \; offsetU = 1 - MU$$
$$offsetL = ML - 1 \quad (3)$$

Where *MU* and *ML* are the upper and lower output modulation indices and δ is the phase difference between them. Fig. shows typical modulating waveforms in the modulation space when the references are not in phase.

3.11 Pulse Width Modulation

Output voltage from an inverter can also be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse-width modulation control used within an inverter [8]. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as Pulse-Width Modulation (PWM) Control synchronous motor drive.

3.12 SPWM Spectra

Although the SPWM waveform has harmonics of several orders in the phase voltage waveform, the dominant ones other than the fundamental are of order n and n±2 where n = fc/fm. This is evident for the spectrum for n=15 and m = 0.8 shown in Fig.5. Note that if the other two phases are identically generated but 120o apart in phase,

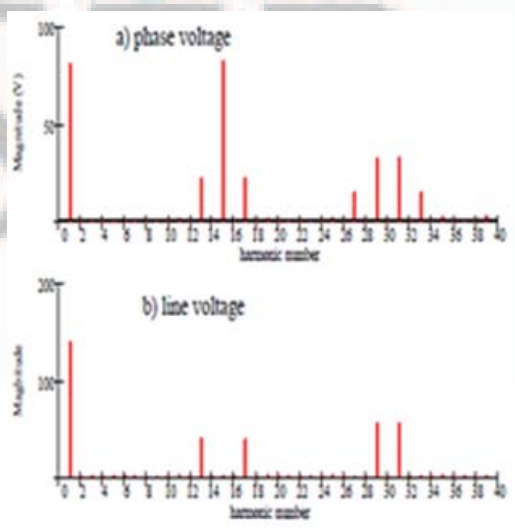

Figure 9: spwm harmonic spectra

The line-line voltage will not have any triplen harmonics. Hence it is advisable to choose, as then the dominant harmonic [7] will be eliminated. It is evident from Fig 5b, that the dominant 15th harmonic in Fig. 5a is effectively eliminated in the line voltage. Choosing a multiple of 3 is also convenient as then the same triangular Waveform can be used as the carrier in all three phases, leading to some simplification in hardware. It is readily seen that as the where E is the dc bus voltage, that the rms value of the output voltage signal is unaffected by the PWM process. This is strictly true for the phase voltage as triplen harmonic orders are cancelled in the line voltage. However, the problematic harmonics are shifted to higher orders, thereby making filtering much easier. Often, the filtering is carried out via the natural high-impedance characteristic of the load.

4. Conclusion

Dual-leg and single-leg reduced switch count dual-output inverter topologies based on three-switch inverter legs were proposed in this paper with the aim of reducing cost, size, and weight of low-power inverters. The performance of the proposed topologies was compared to the conventional topologies regarding the output waveform characteristics and semiconductor power losses. Two prototypes of the proposed inverters were built and tested and the validating results were provided to confirm the discussed issues.

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