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Design of Fast Transient Low-Dropout Voltage Regulator with an Error Amplifier

V. Nandhini[1], D. Yasar Arfath[2]

[1]PG Student, Department of ECE, Karpagam University, Coimbatore, Tamilnadu, India
[2]Professor, Department of ECE, Karpagam University, Coimbatore, Tamilnadu, India

Abstract: ***This paper presents a Low dropout voltage regulator with an error amplifier, which eliminates the use of large capacitors in the output of the regulator. The use of error amplifier reduces the error voltage and improves the transient response of the LDO regulator. The proposed circuit was implemented with a power supply voltage of 1.8V in 0.18µm standard technology. The LDO circuit consumes a quiescent current of 12.2mA with a dropout voltage of 200mV. The proposed LDO architecture supports higher load transients and provides stability when used in analog circuits.***

Keywords: Compensating circuit, dropout, offset voltage, transient response.

1. Introduction

A linear voltage regulator operates at a small input-output differential voltage is called as low dropout voltage regulator. LDO regulators offers lower operating voltage, small active area, higher efficiency and minimum power dissipation. The operation of proposed LDO depends on the error signal produced by the error amplifier, which controls the output current. The importance of designing an error less LDO circuit lies in the fact of increasing demand for high performance power supply circuits. The LDO regulator provides frequency stability for all load conditions, high PSRR performance for a wide frequency range, fast transient response and high current efficiency.

The proposed circuit must respond to sudden changes in both the output current load and the input voltage supply. LDO regulators are used in many applications like automotive, power management and industrial areas, which requires a low dropout voltage for its proper functioning. LDOs are also used in portable devices to power up some of the highly used gadgets like camera, laptops, mobile phones which uses blue-tooth and Wireless frequency applications. LDOs can be categorized into low power and high power LDOs. Low power LDOs produces a minimum current less than 1mA which is used in portable applications. High power LDOs produces a maximum current greater than 1mA which can be used in industrial applications.

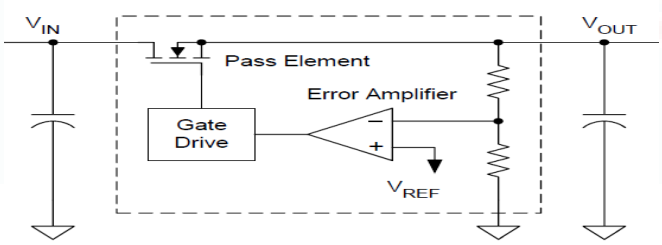

Figure 1: LDO Block Diagram

LDO is the one of the essential element used in any power management unit. Both supply operating voltage and current consumption of the circuits are decreasing to make LDOs applicable in power management units. The operating voltage is an important parameter to be taken into consideration for the new fabrication processes. This decreases dimension and the threshold voltage of the transistors. As a result of low voltage and low quiescent current LDOs can be preferred to be used in SoC applications.

2. LDO Architecture

The proposed LDO circuit consists of two stages. First stage is the error amplifier, which compares reference voltage with the feedback voltage and amplifies the difference to reduce the error voltage. If the feedback voltage is lower than the reference voltage, the gate of the pass transistor allows more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the pass transistor restricts the current flow and decreasing the output voltage.

Second stage is the compensating network, which consists of feedback voltage divider and a pass transistor. The magnitude of the input voltage is greater than output voltage, which gives a better performance. The error amplifier is a differential pair with three current mirror amplifiers M_0-M_3 and M_e. The error amplifier gain ranges between 40 and 50 dB. The error amplifier can, therefore, be designed to meet desired parameters such as the output noise, power consumption, and dc gain. The structure of the proposed LDO circuit is given in Figure 2.

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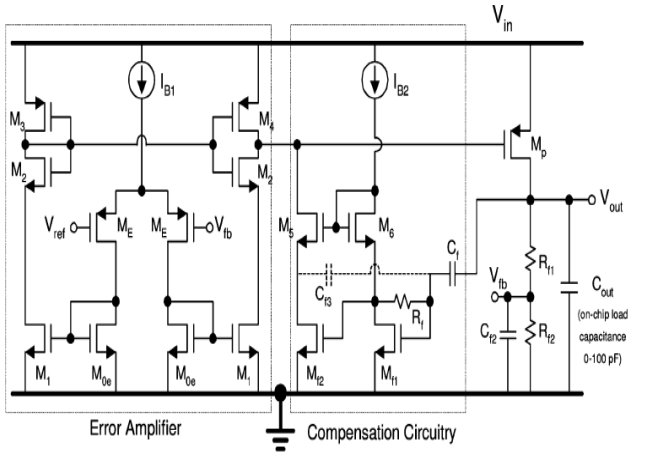

Figure 2: Circuit Diagram of proposed LDO regulator

The output accuracy of the proposed LDO is high due to two pair of current mirrors that require good matching (M_2-M_3 and M_4-M_2). The offset voltage due to large variations at the error amplifier output is reduced in the proposed LDO due to the gain stage formed by M_p. The output noise of the proposed LDO is low and no coupling noise is imposed on the error amplifier. Moreover, the output noise from the error amplifier can be minimized by large Trans-conductance of amplifier.

The power transistor (M_p) operates in saturation region in the LDO regulator. The voltage gain of the power transistor M_p is less than unity and the gain is not decreased due to the error amplifier and compensating circuit. In the proposed design the loop gain is more than 60dB and gives good load regulations. Due to cascade architecture, the loop gain depends on the products of the voltage gains of the two gain stages. The high loop gain provides good line and load regulations. The schematic of the proposed LDO regulator is given in Figure 3.

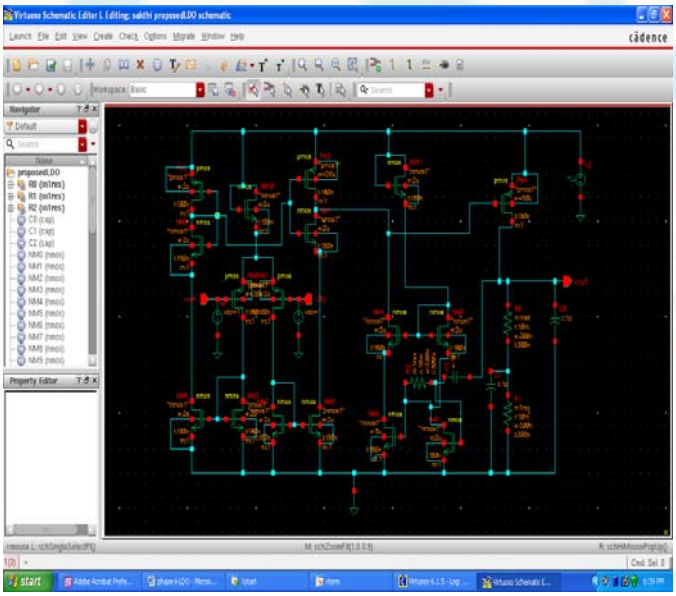

Figure 3: Schematic of proposed LDO regulator

3. Experimental Results

The proposed LDO regulator was fabricated using the 0.18-µm. The LDO regulator uses 1.8V MOS transistors; therefore, the maximum operation voltage is 1.8 V. Fig. 4 shows the input resistance and output voltage characteristics of LDO regulator. The dropout voltage is 200 mV. Fig. 5 shows the input and output voltage characteristics of LDO regulator. The supply voltage switches between 1.8 and 2.5 V with 200 mA output current. Fig. 6 shows the time and current characteristics of LDO regulator. The output current varies from 0 to 200 mA at 1.8 V supply voltage. Table I describes the design parameter values of transistors employed in the proposed LDO regulator.

The load transient voltage spike is only 2V. The quiescent current of 12.2 µA was measured with a load current I_{OUT} = 200 mA. All bias current flows into the ground and the current flowing into the ground pin is measured as the quiescent current. The current efficiency was obtained from (1).

$$\eta I = \frac{I_{OUT}}{I_{GND} + I_{OUT}} \quad (1)$$

$$= \frac{150\ mA}{12.2\ \mu A + 150\ mA}$$

$$= 99.97\%$$

Table I: Design parameter values

.	W(µm)	L(µm)	I_D(µA)
M_E	20	2	2.5
M_{0e}	1	2	2.5
M_1	2	2	5
M_2	5	2	5
M_3	2.9	2	5
M_4	20.3	2	35
M_5, M_{f2}	3	0.4	30
M_6, M_{f1}	1	0.4	10
M_P	16000	0.4	10

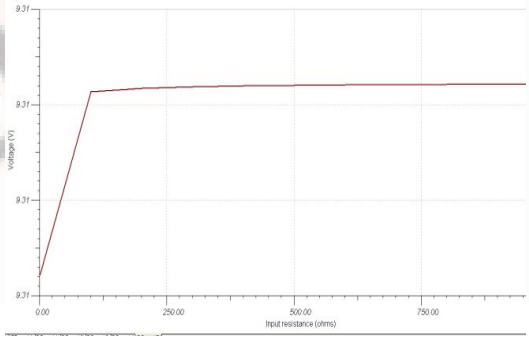

Figure 4: Input Resistance Vs Output Voltage

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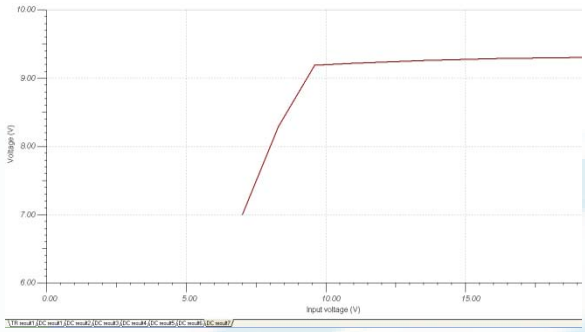

Figure 5: Input Voltage Vs Output Voltage

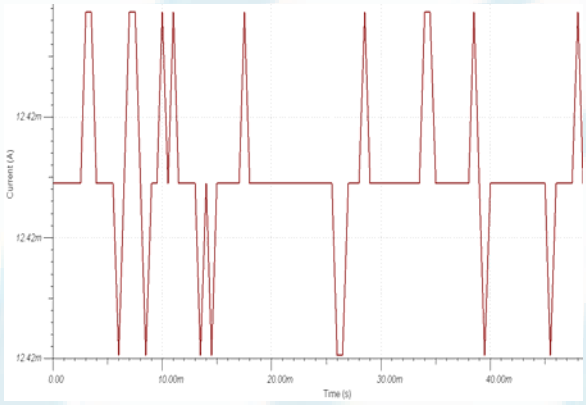

Figure 6: Time Vs Current

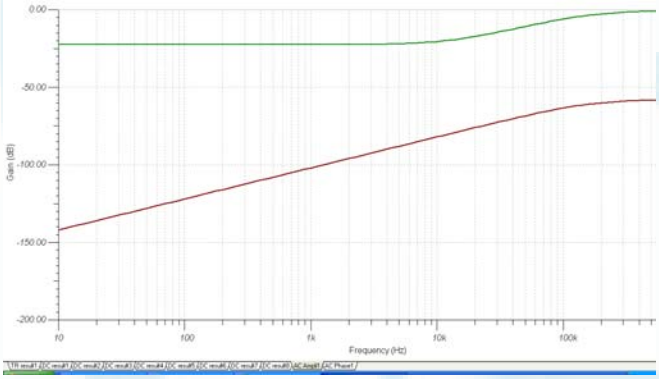

Figure 7: Gain Plot (Frequency Vs Gain)

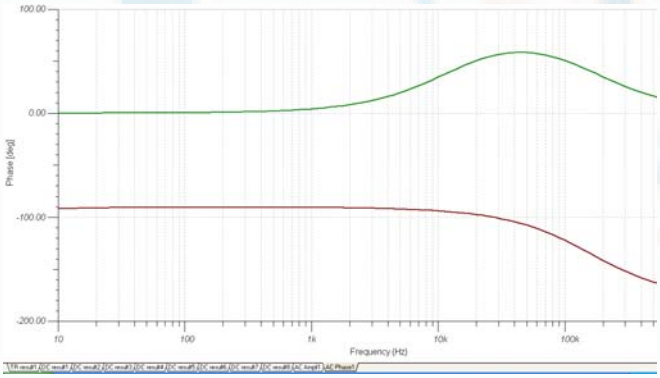

Figure 8: Phase Plot (Frequency Vs Phase)

Fig. 7 and Fig. 8 show the gain plot and phase plot of LDO regulator. Performance comparison between previously reported LDOs and the proposed LDO is summarized in Table II.

Table II: Comparison of parameters

PARAMETERS	EXISTING	PROPOSED
V_{out}	80mv	2v
I_q	25uA	12.2mA
Technology	350	180
Capacitor	100pf	1uf
Supply voltage	3.3v	1.8v

Therefore, the proposed LDO regulator gives a good static and transient characteristic when compared to the existing LDO regulator [1]. By using 0.18µm CMOS technology, the chip area of the proposed design is smaller than the existing LDO regulator [1].

4. Conclusion

The proposed LDO voltage regulator gives a better performance from the results of both transient response and ac stability which consumes only 12.2m A of quiescent current. This proposed circuit provides stability for ac circuits, consumes low power, but it provides a low dropout voltage and fast settling time. The LDO output change as the instance input bias current changes. The output voltage spike of the LDO of the proposed circuit is 2V when the output current changes from 0 to 200 mA.

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Author Profile

Nandhini.V received the B.Sc. degree in Electronics from P.S.G College of Arts and Science in 2007. She received the M.Sc. degree in Electronics and Communication Systems from Sri Krishna Arts and Science College in 2009. She received the M.Phil. degree in Electronics with specialization of Embedded systems from Sri Krishna Arts and Science College in 2012. At present working as Assistant professor in Department of Electronics and Communication Systems in Sri Krishna Arts and Science College and pursuing M.E in VLSI Design in Karpagam University.

Yasar Arfath. D received the B.E. degree in Electronics and Communication Engineering from Hindusthan College of Engineering and Technology in 2004. He received the M.Tech. degree in Electronics and Communication from IASE University, Rajasthan in 2006. At present working as Assistant professor in Department of Electronics and Communication Engineering in Karpagam University and undergoing his research work.