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Design of a Multi-Standard DUC Based FIR Filter Using VLSI Architecture

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Abstract: ***In Digital Signal Processing FIR Filter is used to remove the noise or unwanted components from a signal. This paper Presents an efficient VLSI Architecture of a Multi-Standard Digital Up Converter (DUC) based FIR filter that is used to remove the noise in the received channel data bits effectively. The proposed DUC based FIR filter consists of weight update block with Shift add architecture to achieve a lower adaptation delay and efficient area, power, delay. In this proposed architecture for achieving an efficient adaptation delay and area-delay-power implementation, shift add architecture is used and to modify the architecture for the implementation of a delayed least mean square (LMS) adaptive filter using three co-efficient inputs. Number of Look Up Table (LUT) counts, path delay time and power consumption are reduced and the results prove that the Proposed technique produces higher speed when compared to the existing DUC based FIR filter architecture.***

Keywords: Finite Impulse Response (FIR) Interpolation filter, Digital Up Converter (DUC), Shift add architecture, Partial Product Generator (PPG).

1. Introduction

VLSI Technology is used to modify the any types of digital based hardware architecture and to reduce the hardware system power, speed and complexity. FIR filter is the most popular digital filter with finite duration. FIR filters are widely used in Digital Up Converter. Digital Up Converter is used to convert the signal sample rate when the signal is transmitted from Base band to Intermediate band. In DUC technique input signal is filtered and converted into higher sampling rate. In digital Signal Processing using numerous sampling rates can improve a software defined radio (SDR) as more flexible.SDR is a single device having different standards for different sample rates, channel bandwidths and carrier-to-noise ratios. This SDR technique helps to make a development of a reconfigurable sample rate converter chip.

In Distributed Arithmetic (DA) based an efficient implementation of FIR filter [1] the multipliers are replaced by multiplierless technique. The performances of various filter orders with various partitions on different length of partial tables are presented. This technique gives very greater potential for high throughput and reduced-latency in implementation but cannot be addressed by the same type of scaled bits of all the input variables.

High speed and area efficient multiplierless architecture [2] for FIR filter is the Lookup table less architecture uses the speed advantage of carry save adder and the time complexity depends only on the input word length, independent of the order of filter but the memory size grows exponentially as the filter order increases.

The Digital Interpolation Systems (DIS) for integer upsampling [3] can be implemented by efficiently measured the number of multiplications required for each output sample point. This technique can be used to take advantage of the symmetric impulse response, and generate a 50% savings in computation but the polyphase technique cannot directly be applied.

The general purposes multipliers [4] of traditional multiply and accumulate [MAC] implementations are replaced by combinational Look Up Table (LUT) blocks. Since LUT blocks can be of considerable size so, the quality of digital filter implementation highly depends on efficiency of logic synthesis algorithm. The Field Programmable Gate Array (FPGA) is to maintain the advantages of custom functionality like an Application Specific Integrated Circuits (ASIC), while preventing the high development costs and the inability to make design modifications after production but the size of Distributed Arithmetic-LUT increases exponentially with the length of input.

The design of low power reconfigurable finite impulse response (LPRFIR) filter [5] is well suited when the filter order is fixed and not changed for specific applications and flexible trade-off between power savings and filter performance was presented. Approximate signal processing techniques are used for the design of low power digital filter order dynamically varies according to the stop band energy of the input signal but once the filter architecture is designed, the coefficients cannot be changed. So, these techniques are not applicable to the FIR filter with programmable coefficients.

An extension to the theoretical lower bounds [6] for the number of adders and their depth in multiplierless single constant multiplications (SCM) that the number of prime factors of the constants is key source to extend the current lower bounds in particular cases. This techniques yields higher performances and lower area, low power consumption at expenses of increasing the number of arithmetic logical operations but does not have the minimum number of cost and depth operations.

A two-step optimization technique [9] for designing a reconfigurable VLSI architecture of an pulse shaping filter for multi-standard digital up converter (DUC) is used to reduce the power and area consumption. This technique

initially reduces the number of multiplications and additions per input samples and a 2-bit binary common subexpression (BCS)-based BCS elimination algorithm to design an efficient constant multiplier. This technique has succeeded in reducing the area and power by along with improvement in operating clock frequency over a 3-bit BCS-based technique.

An efficient power and area architecture of pulse shaping FIR filter [15] for digital up converter was designed. In this design, carry save adder is used instead of shift and add method and also the simple adders of multiplexer unit is replaced by carry save adder. The number of multiplications and additions are reduced using this technique. Therefore, the speed of the operation gets increased and also area of the architecture gets minimized.

2. Design of a Reconfigurable Root-Raised-Cosine (RRC) Fir Filter Architecture

A design of Multi-Standard DUC consists of three basic standards. The standards are wideband code division multiple access (WCDMA), universal mobile telecommunication system (UMTS) and digital video broadcast (DVB).These standards have adopted root-raised-cosine (RRC) filter as pulse shaping filter is used to reduce the bit error rate (BER).

An efficient implementation of a reconfigurable RRC FIR filter architecture consists of different modules, namely Data Generator (DG) Block, a Co-efficient Generator (CG) Block, a Co-efficient Selector (CS) Block and a Final Accumulation (FA) Unit Block. The proposed RRC filter architecture is shown in the Fig.1.

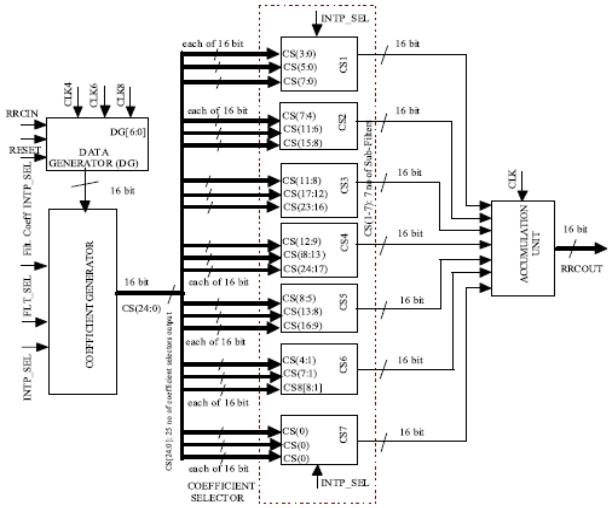

Figure 1: Proposed reconfigurable RRC filter architecture

1. Data Generator (DG) Block

The clock signal is applied to the data generator, it will sample the input data (RRCIN) based on the selection lines of multiplexer parameter (INTP_SEL).

2. Coefficient Generator (CG) Block

Coefficient Generator consists of first coding pass, second coding pass, Shift and add architecture, multiplexer unit and addition unit is shown in the Fig.2.The multiplication operation between the inputs and the filter coefficients is performed by the coefficient generator (CG). The hardware has been reduced by two-phase optimization technique. Each of the blocks in the Coefficient Generator is structured using multiplexer.

2. a. First Coding Pass: The output of the data generator blocks are taken as inputs of the First Coding Pass (FCP) block are processed and then based on the selected values of the selection lines of multiplexer the FCP outputs are produced.

2. b. Second Coding Pass: The operation of this block is similar to the FCP. The outputs from the FCP block are taken as the input of this Second Coding Pass (SCP) block are processed and based on the selected values of the selection lines of multiplexer the SCP outputs are produced.

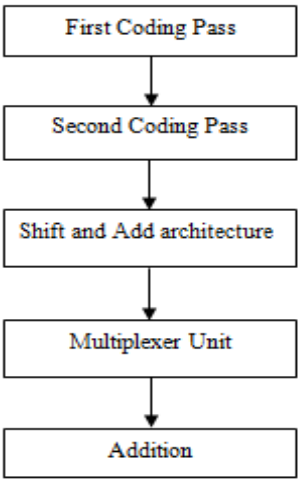

Figure 2: Data flow diagram of proposed CG Block

2. c. Shift and Add Architecture: Shift add architecture is used to generate the partial products. It is a design of 8 bit shift add architecture and 16-bit partial product generator architecture. This two architecture used to the filtering process.

The 8-bit shift add architecture is used to add two 8-bit values and this addition process is mainly focused by tree based addition technique and to reduce the carry selection process.

The 16-bit partial product generator (PPG) architecture is used to add the original bits and the desired bits. This PPG unit is to optimize the multiplier architecture level. So that the delay can be reduced and the speed has been increased.

2. d. Multiplexer Unit: The output of shift add architecture is given as the inputs to the multiplexer. It will choose the required data from the shift add architecture based on the coded coefficients. The selected inputs are processed and the outputs that are produced from the multiplexer unit are again summed up with shift add architecture.

2. e. Addition Unit: The inputs are taken as the output of eight multiplexer units. The output of the eight multiplexers (M7-M0) is added together. The outputs of the adder passes through a two's complement circuit. The produced outputs are varies depending on the sign magnitude and then given to the multiplexer and the outputs are produced.

3. Coefficient Selector (CS) Block

The inputs are taken from the output of the coefficient generator which selects the required data for processing and the selected inputs are multiplied using the AND operation and then based on the multiplexer's selection line, outputs will be produced.

4. Final Data Accumulation Unit (FA)

The inputs for accumulation were taken from the output of the data generator (DG), coefficient generator (CG) and coefficient selector (CS) which are added and then filter output will be produced.

3. Simulation and Results

Finally the 16-bit channel based FIR filter digital architecture was designed. This architecture is used to reduce the noise level in received signal. Then to simulate the final output binary results and to calculate the circuit complexity, power and the speed level.The proposed design has been simulated on ISIM using Xilinx ISE 14.2.The binary data inputs are given and corresponding clock signal is applied either 0 or 1.The waveform are generated to their corresponding inputs. The simulation outputs of the proposed RRC filter architecture is shown in the Fig.3.a and Fig.3.b.

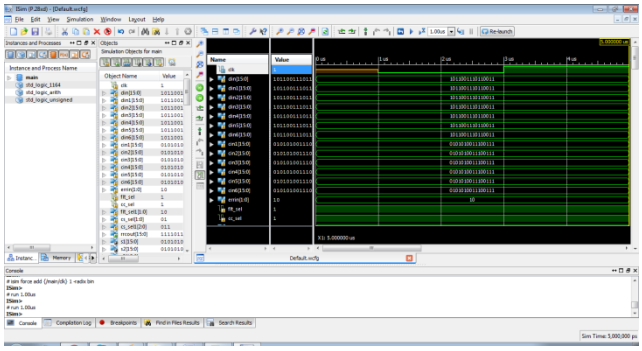

Figure 3.a: Simulation inputs of the proposed reconfigurable RRC filter architecture

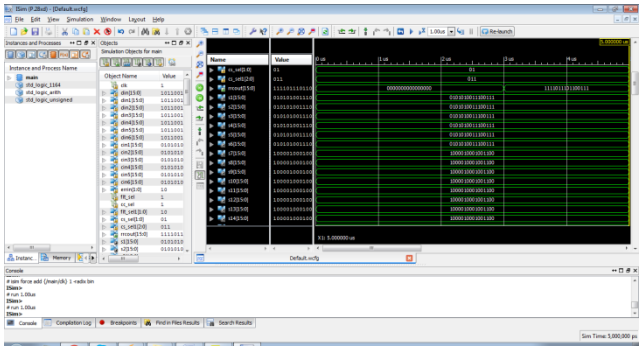

Figure 3.b: Simulation outputs of the proposed reconfigurable RRC filter

After simulation process the proposed design has been implemented using Xilinx ISE 14.2.The Register Transfer Level (RTL) diagram can be implemented for the proposed RRC filter. The simulation and Synthesis Report shows that an efficient Area-Power-delay utilization. The RTL Schematic view of the reconfigurable RRC filter architecture is shown in the Fig.3.c.

Fig.3.c: RTL Schematic view of reconfigurable RRC filter

Total on-chip power as both static and dynamic power can be measured by using Xilinx Power Estimator (XPE)-2013.3.Comparison have been done for the power, delay time, LUT counts and clock frequency of the proposed reconfigurable RRC filter architecture.

Table I: Comparison results of the [9] and proposed reconfigurable RRC filter

References	*LUT counts*	*Delay Time(ns)*	*Maximum .Frequency(MHz)*	*Power (mW)*
[9]	3142	11.9	83.4	231.21
Proposed	2135	9.102	109.8	208

From Table I, it is noticed that the proposed technique helps in reducing LUT counts, Delay time and power along with improvement of maximum frequency compared with [9] existing technique.

4. Conclusion

Finally the FIR with DUC multi-standard channel filter architecture was designed. The circuit complexity level and the delay were reduced. This FIR filter architecture is used to remove the noise in the received channel data bits effectively. This architecture addresses different problems encountered in designing the reconfigurable filter used in multi-standard DUC, which is an important component of Software Defined Radio /cognitive radio. Number of Look Up Table (LUT) counts, path delay and power. This two-step optimization technique to make the desired filter more efficient by reducing area and power along with improvement in operating clock frequency of the design. Comparisons of results of the proposed architecture with other reconfigurable FIR filter architecture implemented on FPGA demonstrate merits of the proposed architecture in terms of speed, power, and area consumption compared to the existing reconfigurable RRC filter architecture. Further the reconfigurable RRC filter architecture is to be enhanced along with an efficient power and area.

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