

Developing Throughput in Associative Memory Using Phase Overlapped Processing Scheme

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Abstract: A Content Addressable Memory (CAM) is a special sort of search memory utilized in high speed seeking appliance. This paper establishes a Phase overlapped processing scheme to increase the throughput and low energy content addressable memories. Traditionally, the power consumption in CAMs due to high switching activity is considered as the main limiting factor in CAM. In order to diminish the switching activity of the Memory Cell in Binary Content Addressable Memory (BCAM), 10T SRAM is implemented and also introduces a power consumption minimization technique for Ternary Content Addressable Memories (TCAMs) which are used mainly for high-speed packet transmission and classification over routers and switches in network. The self-timed word circuit is independently manipulated by a locally generated control signal, it reducing the power dissipation of global clocking. This tolerates the circuits to be in the necessary phase for their individual local operation contains evaluate or precharge, which enormously diminish the cycle time. As, a design example, CAM is implemented and evaluated by Tanner simulation under a 130 nm CMOS technology.

Keywords: CAM, Precharge phase, Evaluate phase, SRAM Cell, NAND cell, BCAM, TCAM, Asynchronous clock signal.

1. Introduction

Content-Addressable memories (CAMs) are used in high speed search engines that are much faster than other approaches utilized for search-exhaustive applications. There are two basic types of CAM: Binary CAM (BCAM) and Ternary CAM (TCAM). Binary CAMs maintain storage and penetrating of binary bits, it allows only zero or one (0,1). The TCAMs are capable of storing and searching ternary states ('0', '1', and 'X'). In a search operation, the 'X' state can be used as a wild card. An input search word is compared with a table of stored words and the matching word is obtained at high speed through a parallel equality search.

However, the area and power of a CAM is the main factor for speed approach at the cost of augmented silicon area, the designers are struggle to reduce these two parameters. As CAM applications produces, demanding larger CAM sizes, the power difficulty is further exacerbated. Diminishing power utilization, without sacrificing speed or area, is the most important thread of recent research in huge capacity CAMs. In this paper, a Phase overlapped processing scheme (POP) for increase the throughput and low-energy CAM is introduced. In a CAM, most mismatches can be found by investigating a few given bits with the stored word of the circuit.

CAMs often contain a few hundred to 32 K entries for network routers. Each input-search bit is compared with its CAM-cell bit and the comparison result determines whether a pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on or off states. CAM cells are classified into two types: NOR and NAND. In contrast, a NAND-type word circuit operates at medium speed because pass transistors are connected serially between a ML to a ground line. Because very few matched word circuits discharge their ML capacitances, a

NAND-type word circuit reduces the power dissipation of MLs compared to the NOR-type word circuit.

This paper presents a Pai-Sigma match line based synchronous and self-timed circuits in order to reduce the search power of TCAMs. The proposed methodology can overcome from the issues such as charge sharing and short circuit current. The remainder of this paper is sorted as follows. Section 2 describes the operation of Content Addressable Memory. Section 3 reviews the power reduction techniques of BCAMs. Section 4 presents the architecture of the proposed Pai Sigma match line based self-timed circuits. Section 5 deals with the simulation results and discussion. Finally, section 6 concludes the paper with main points and future directions.

2. Basics of Content Addressable Memory

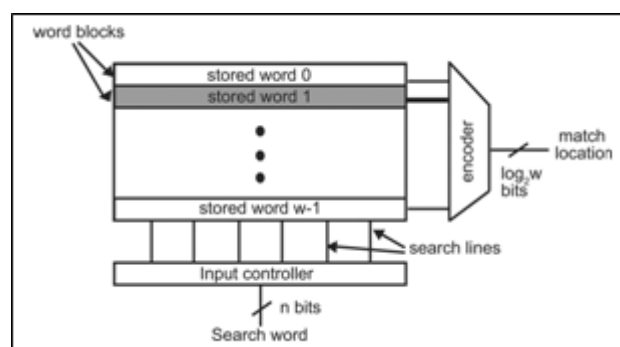


Figure 1: Block diagram of content addressable memory

Fig. 1 shows a block diagram of a CAM. A search word is broadcast onto search lines (SLs) to the table of stored words whose sizes are n bits. The amount of bits in a CAM word circuit typically sorts from 36 to 144 bits. A typical CAM utilizes a table size sorting between a small amount of hundred entries to 32 K entries. Each word block has a match line (ML) that indicates whether search and stored words are the same or different. The outputs from the word blocks are given to an encoder that produces a

binary match location i.e., 0 or 1 corresponding to the ML that is in the match state.

The storage and comparison are performed in the CAM core cells circuitry. The search lines of the CAM run vertically in the figure and transmit the search data to the CAM cells. The match lines run parallelly across the array and designate whether the explore data contest the row's word. If a match line is activated it indicates a match and if it is deactivated match line show a non-match process, called a mismatch.

The search operation in the CAM starts with precharging all match lines high, putting them all provisionally in the match state. Then, the search line constrains broadcast the search data. Next, every CAM core cell search the given data into the stored data. If the search data is matched with the stored data then the matchline remains high, if it is mismatched with the data then the matchline low. The entire results are pulled down the matchlines for any given word that has a minimum of one mismatch. The match lines of the matched data in the cell remain high, indicating a match, while the other match lines in the cell discharge the matchline to ground, reporting a mismatch operation. At last, the encoder produces the location of search address of the contesting data.

3. Design of Binary CAM using POP Scheme

A CAM is a search memory that executes the lookup-table operation utilizing devoted comparison circuitry within a single clock cycle. Phase overlapped processing scheme (POP) is used for increase throughput and low-energy CAM. The POP eases the restriction of the throughput based on overlaps precharge and evaluate phases in dynamic circuits using independent control of word circuits, eliminating the waste time of precharging..

The CAM word circuit is designed based on dynamic logic that contains evaluate and precharge phases. It is normally used in a CAM to reduce its area. Once a search word matches a stored word in an evaluate phase, the ML of the word circuit needs to be pre-charged before the next-word search. In a traditional synchronous CAM, all word circuits are controlled by a global clock signal and hence they periodically operate using two phases. In contrast, in the proposed POP scheme, each word circuit is designed using asynchronous circuits. As each word circuit is independently controlled using its local control signal, unused word circuits are on the evaluate phase, while the others are on the precharge phase. In combination with the RWOS scheme, input search words match in unused different word circuits whose MLs have already been pre-charged. Therefore, new search words are immediately processed without wasting the precharge time.

3.1 SRAM NAND Cell

The Conventional Static Access Memory (SRAM) cell has Six MOS transistors. In the Dynamic RAM (DRAM), the bits are requiring to be refreshed periodically it doesn't need in the SRAM. The importance of SRAM cell, it works at a low level supply voltages and has great noise immunity. It

maintains to play a pivotal function in almost every VLSI systems because its high speed and complete compatibility by means of logic method technology. However as the technology extending persists, SRAM design is facing harsh dare in sustaining enough cell steady margin beneath inexorable area sizing. In order to reduce the switching activity of the circuit the 10T SRAM cell is used.

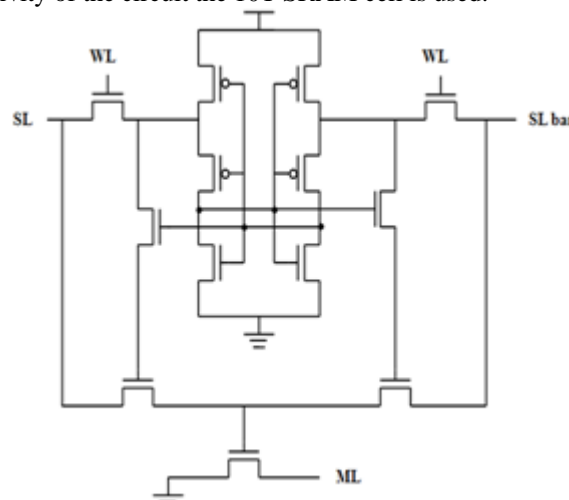


Figure 2 10T SRAM cell

The block diagrams of a typical word circuit based on a NAND-type cell is shown in Fig.2. The NAND type word circuit is implemented using a series of pass transistors in the NAND type cells. It operates in two phases: precharge and evaluate, based on dynamic logic. A word line (WL) is high to write words into the cells, and is low in the search operation. In the write operation, words are stored using complementary signals (BL , \overline{BL}) on bit lines (BLs). Here, the access transistors are connected to pseudo nodes (i.e. nodes between two pull-up transistors) rather than the storage nodes. Due to this, the storage nodes are isolated from the BLs and therefore during the read operation, the read current does not flow through the storage nodes and hence maintain the read constancy. In case of the write operation, the VGND is connected to VDD and one of the bit-lines is grounded. Suppose the first node is storing '1' and the other node is storing '0'. When a high supply voltage is provided, the first node is pulled down to '0' due to discharging through the access and the pull-up transistor. In the search operation (evaluate phase), search words are assigned using complementary signals (SL , \overline{SL}) and compare with their stored words. When a search word is the same as a stored word, the pass transistor connected to the ML is in an on state.

3.2 Phase Overlapped Processing

The Phase overlapped Processing Scheme operates in two phases: precharge and evaluate, based on dynamic logic. In the precharge phase, the Match line in the circuit is charged through the PMOS transistor. In the evaluate phase, the given search word is matched with the stored word all pass transistors in the CAM cells are in on states. Hence, the Match line capacitance is discharged. This process is described as a "match" operation. Suppose, the given search word is different from a stored word, all pass transistors in

the CAM cells are not in on states. Hence, the voltage of the Match Line (ML) remains high. The operation is described as a “mismatch.” The NAND-type word circuit diminishes the power dissipation of MLs contrast with the NOR-type one for the reason that only a matched circuit discharges the ML capacitance.

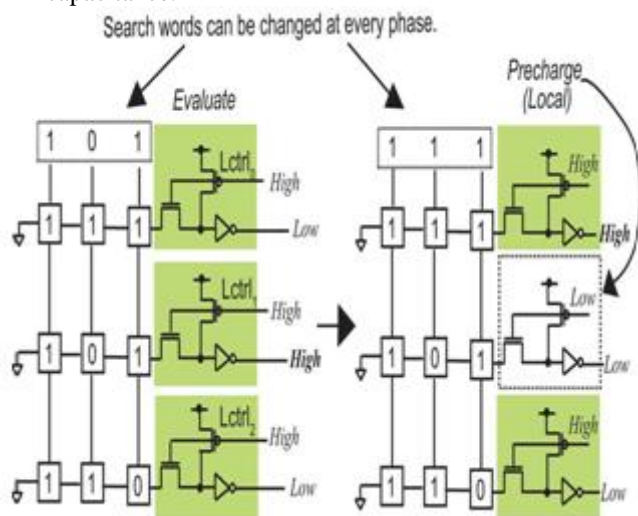


Figure 3: Self-Timed Word Circuit

Figure 3 illustrates the block diagram of the self-timed word circuits based on the Phase Overlapped Processing (POP) scheme. The local clock signal is used in the Phase Overlapped Processing scheme. Here the given word circuit is independently asynchronously and controlled using its own local control signal (lctrl). Every lctrl is independently modified depending on the circumstance of its word circuit, where the local clock is low in a precharge phase and clock is

high in an evaluate phase. In the POP scheme, initially all the match lines(ML) are charged using the lctrl signal in the precharge phase. If a given search word is compared with the stored word then the matched word circuit alone discharged and in the next precharge phase, the discharged Match lines get charged by a lctrl signal and the remaining Match lines are stays high. Using the Word Overlapped search scheme, successive search words are allocated to unused different word circuits that are in an evaluate phase. Therefore the input search words can be processed without squandering the precharge time.

4. Design of Ternary CAM using POP Scheme

TCAM is used in high-speed parallel search operations leads to very high power consumption. To reduce the power consumption of the CAM word circuit, many methods on low power design of TCAM is accounted. In [8], the authors suggested a current-race matchline sensing scheme, it diminish the power consumption by reducing switching activity of the search lines and the voltage swing of the match lines are shrunk. In [1], [4], a matchline is divided into two parts, the first element is an NAND-type matchline and the second element is an NOR-type matchline. Similarly, the comparison result of the initial part decides whether the second part is precharged or not. In a ripple-

precharge matchline scheme which is similar to an NAND-NOR matchline scheme was recommended to diminish the power dissipation of a TCAM.

To attain the concession between the power and the delay of a matchline[1],[4],[5] by using the Hybrid NAND-NOR matchline is one preferred design approach. If the CAM executes a Compare operation, all the NAND type matchlines are activated. But, only the NOR type matchlines with the corresponding NAND matchlines producing a match result are activated. Since the switching power of the NAND matchline is reduced and only a little amount of NOR type matchlines are activated, the compare power of the CAM with NAND-NOR matchlines can radically be diminished. In addition to the delay of the NAND-NOR matchline is improved than that of the NAND matchline. Hence the major disadvantages of the NAND/NOR matchline structures 1) the matchline acquires short circuit current (ie., DC current), it is due to the search results of NAND and NOR matchlines are match and miss, 2) the problem of charge sharing exist in the NAND type matchline process during the search result of the NAND matchline is mismatch. The pulsed NAND-NOR matchline scheme [9] uses a replica matchline to overcome the problem of short current. But the additional area cost and the process variation of the replica matchline will degrade the usefulness of short circuit reduction. Hence, the problem of charge sharing is reduced by the search lines should be precharged to Vdd when the NAND matchline executes the precharge operation. The results of this technique increase the power dissipation of the search lines.

4.1 Pai-Sigma matchline

Figure 4 shows the transistor-level diagram of the proposed Pai-Sigma matchline scheme. The pai sigma matchline reduces the problems in the NAND and NOR type TCAM cells. The pai segment utilizes the NAND function and the sigma segment utilizes the NOR function. Then the two segment is merged with the interface logic between the pai and sigma segment.

In the Precharge phase, the signal pre turns out to be low (ie, pre=0) all the internal nodes of the circuit between the logic can be charged to Vdd or Vdd-Vt. If $(S_i, M_i) = (1, 1), (0, 1), (1, 0)$ then the internal nodes $I_{i+1} = I_i$. Suppose the signal $(S_i, M_i) = (0, 0)$, then the pMOS transistors controlled by S_i and M_i turn on the internal nodes and precharged to logic 1. Hence the search lines of the cells in the pai segment not need to be reset to assure the all internal nodes is precharged to logic 1 and also the ML_{NAND} is precharged to logic 1 through pMOS transistor. This can eliminate the problem of short circuit current in the interface logic and the dynamic power. In the evaluate phase (pre = 1), both S_i and M_i of the pai segment are not logic 0, i.e., the search result is match, then the ML_{NAND} and the internal nodes produce logic 0. If any of the S_i and M_i goes to logic, i.e., the search result is mismatch, then the corresponding pMOS transistors are turned on and the internal nodes I_{i+1} are precharged to logic 1. Hence, it is propagated to

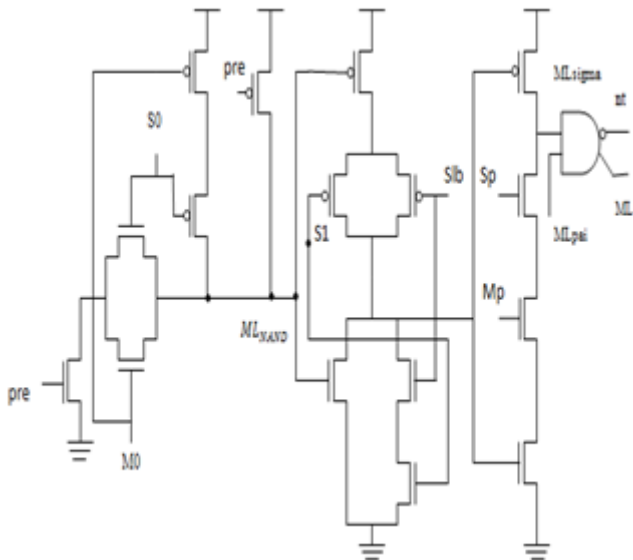


Figure 4: Structure Of Pai-Sigma Matchline

the consecutive internal nodes through the nMOS transistor. The interface logic uses the static CMOS gate to cascade the NAND and the NOR match line to eliminate charge sharing. The input to the static CMOS gate depends on the Si, Mi and ML_{NAND} . Therefore, if the search result of the cell in the pai segment is in match, then the interface logic produces a logic 1 at ML_{pai} node. Then, the precharged pMOS of the NOR matchline will be turned off. The short circuit path does not exist, If the search result of NOR matchline is miss. The final result of the matchline (ML) is active, when the ML_{pai} and the ML_{sigma} produces logic 1. The truth table of the ML with respect to ML_{NAND} , ML_{pai} , ML_{sigma} is shown in the Table I.

Table 1: Truth Table

ML_{NAND}	ML_{pai}	ML_{sigma}	ML
1	0	1	0 (Mismatch)
0	0	1	0 (Mismatch)
0	1	0	0 (Mismatch)
0	1	1	1 (Match)

4.2 POP based on Pai-Sigma Matchline

Figure 6 illustrates the block diagram of the self-timed word circuits based on the Phase Overlapped Processing (POP) scheme. Here the given word circuit is independently asynchronously and controlled using its own local control signal (Ictrl). In the POP scheme, initially all the match lines(ML) are charged using the Ictrl signal in the precharge phase. If a given search word is compared with the stored word then the matched word circuit alone discharged and in the next precharge phase, the discharged Match lines get charged by a Ictrl signal and the remaining Match lines are stays high.

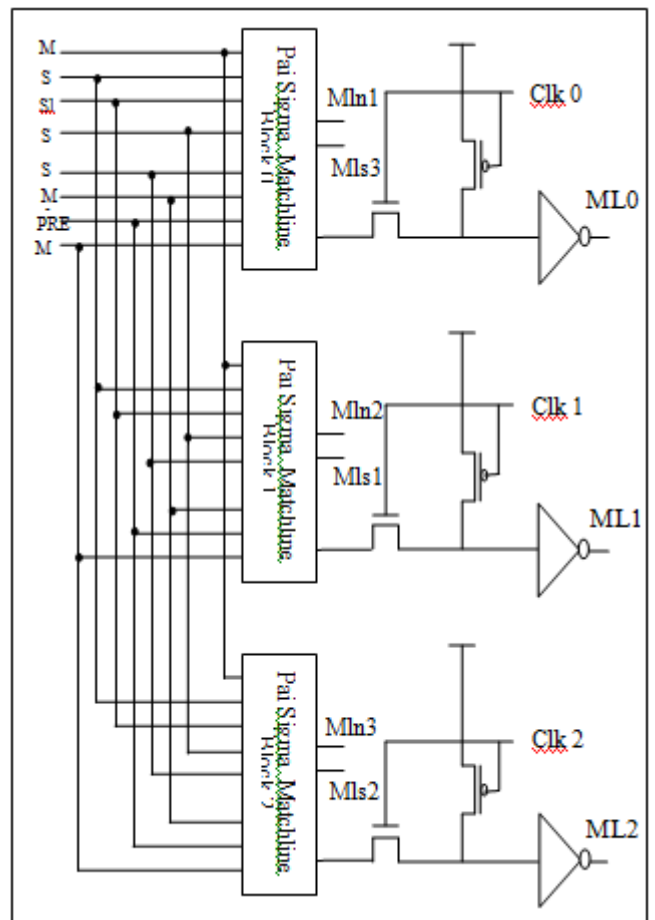


Fig. 5. POP Scheme word circuit based on Pai-Sigma matchline

5. Results and Inference

In the content addressable memory, the select line is used to select the bit according to the input given to the memory. The output will depend on the match line. Tanner EDA is to design the memory, the output waveform, power, leakage current is determined using T-Spice.

5.1 NAND Cell

The NAND cell is used to store a 1 bit data in the memory because it reduces the power dissipation of (Match lines) MLs compared to the NOR-type word circuit. In order to reduce the switching activity of the memory the 10T SRAM is used. The Power of the cell is described below. The Power consumed in the circuit is determined using Tanner Spice and the Power is decreased by reducing the switching activity of the cell.

TABLE II involves the parameter used to describe the circuit performance and shows that the power is diminished compare with traditional SRAM Cell.

Table 2: Power Analysis

NAND cell	Average power consumption (W)	Leakage current(A)
Existing 6T SRAM	0.1059 m	58.67 u
Proposed 10T SRAM	0.08510 m	47.27 u

5.2 Output Waveform of BCAM

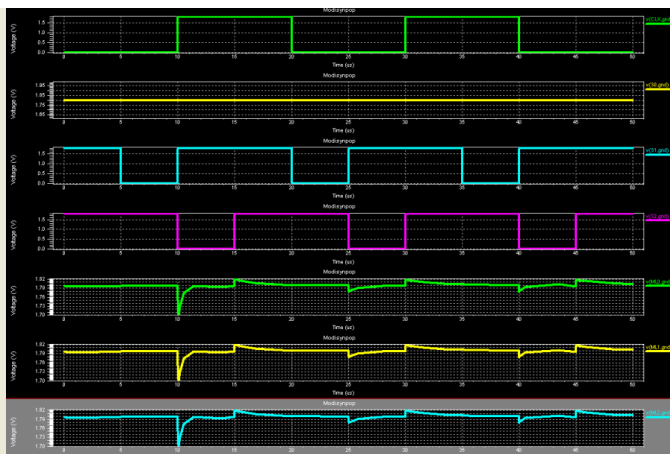


Figure 7: BCAM Output using asynchronous signal

The inputs to the CAM word circuit based on POP scheme are Search Lines (S0, S1, S2) represented in yellow_1, blue_1 and pink which are used to provide search data. The results are verified from the waveform obtained in the W-Edit. Hence, the resultant value is obtained in Match Line (ML0, ML1, ML2) represented in green, yellow_2 and blue_2. The ML2 value shows the result of comparison whether match or mismatch of each row.

The Comparison TABLE III describes the performance of the proposed method compared with existing method. The power is diminished because, during the Read operation, the current does not flow through the storage node, it maintains the read stability of the circuit. The leakage current is reduced because the voltage applied to the pull up transistor is high and the voltage for access transistor is low and also it increases the speed for storing the data in the cell.

Table 3: Parameter Comparison of Existing Vs Proposed BCAM

CAM using Asynchronous signal	Average power Consumption (W)	Leakage Current(A)
Existing method	5.724m	3.18m
Proposed method	5.114m	2.841m

5.3 Output Waveform of TCAM

Figure 8 illustrates the waveform of pai-sigma based POP scheme. In the precharge phase all the matchlines are low and in the evaluate phase, the matchlines are turns out to be 1.

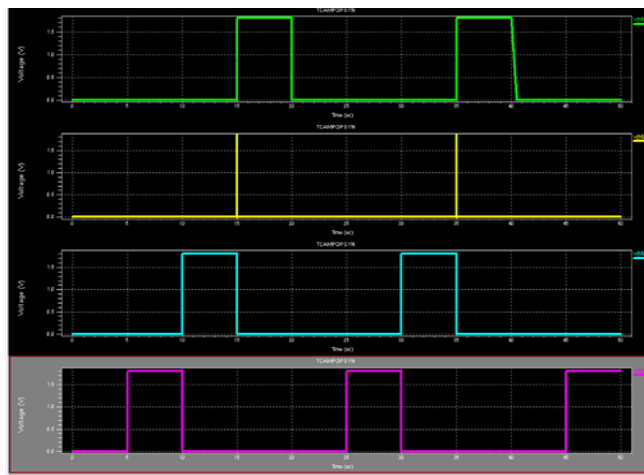


Figure 8: TCAM Output using POP based on Pai-Sigma matchline

Table IV summarizes the comparison results of the proposed low-power TCAM based on overlapped search mechanism and existing low-power BCAM. The performance parameters are calculated in order to determine the efficiency of CAM. The static current which are the power consumed and current drawn because of the switching activities in CAM. The area represents the space occupied by the transistors in CAM. From the comparison table, it can be seen that the power consumption for the proposed TCAM in combination with synchronous control and POP scheme dissipates less power when compared to the existing BCAM in combination with synchronous control and POP scheme.

Table 4: Parameter Comparison of Existing Vs Proposed TCAM

Performance Parameters	POP Scheme (BCAM)	POP Scheme (TCAM)
Dynamic power (Watts)	0.05u	0.03u
Static power (Watts)	8.90 m	8.7 m
Static current (Amps)	4.91 m	4.5 m
Area (μm^2)	675	487.5

6. Conclusion

The project described the design of asynchronous high throughput Content Addressable Memory that stores a single bit using 10T SRAM. Memory cell is designed and the local control signal is used to enable the cell during Precharge Phase and the design of asynchronous low power TCAM using the Pai-Sigma matchline scheme which does not suffer from the problems of charge sharing and the DC path does not exist by inserting the additional timing signal.. At the circuit level, the Phase overlapped Processing (POP) hides the delay of a precharge phase using local control and hence greatly reduces the cycle time compared with a traditional synchronous scheme. The simulation results confirmed that the proposed CAM can effectively save the Power and increase the efficiency by reducing the number of switching activity of the cell.

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