International Journal of Scientific Engineering and Research (IJSER)
www.ijser.in
ISSN (Online): 2347-3878, Impact Factor (2014): 3.05

Enhancement of Power Quality by Using MC-UPQC

D. Subba Rao[1], T. Srinivasa Rao[2]

[1]Assistant Professor, Electrical & Electronics Engineering KKR&KSR Institute of Technology & Sciences, Vinjanampadu, Guntur-522017, India

[2]Professor& HOD, Electrical & Electronics Engineering, KKR&KSR Institute of Technology & Sciences, Vinjanampadu, Guntur-522017, India

Abstract: ***This paper presents a power quality improvement by using multi converter unified power-quality conditioning system (MC-UPQC), it will provide the following multi functions: reactive power compensation, harmonic compensation, flicker/ imbalance compensation and voltage sag/swell in multi bus/multi feeder systems. With this topology the supply voltage fluctuations on both feeders and current fluctuations on main feeder is compensated. In this system the three VSCs are connected back to back with a common dc-link capacitor. Sag/swell and interruption are compensated by transferring the power from one feeder to another feeder.***

Keywords: Power quality (PQ), Unified power quality conditioner (UPQC), MATLAB/SIMULINK, Voltage Source Converter (VSC), Voltage sag, Voltage swell.

1. Introduction

With significant development of power electronics technology, the proliferation of nonlinear loads such as static power converters has deteriorated power quality in power transmission/distribution systems. Notably, voltage harmonics resulting from current harmonics produced by the nonlinear loads have become a serious problem in many countries [1].Active filtering is used to meet the PQ in standard limits [2].Series and shunt active power filters are used to compensate the voltage imperfections and negative load effect on supply system [3].The UPFC concept provides a powerful tool for the cost effective utilization of individual transmission lines by facilitating the independent control of both the real and reactive power flow, and thus the maximization of real power transfer at minimum losses, in the line [4].When the power flow is controlled multiline by using IPFC and GUPFC.

The GUPFC consisting of three converters, one connected in shunt and the other two in series with two transmission lines exiting a substation is considered. The GUPFC extends the concept of power and voltage control beyond that achievable with the known two converter UPFC and IPFC FACTS controllers. The GUPFC is capable of providing voltage control at a bus as well as independent real and reactive power flow control on two transmission lines therefore controlling a total of five power system quantities. Two-converter applications each provide control capability for three power system quantities. The addition of the third converter provides 2 more degrees of freedom in control of power systems. The GUPFC is increases the power flow capability and also control the voltage fluctuations when it is installed in some central substation. The GUPFC not only increases the power flow, it also decreases with respect to operating conditions. In general, the GUPFC can be used to increase the transfer capability and relieve congestions in a flexible way.

The IUPQC is design for PQ improvement in adjacent feeders. The IUPQC has two converters those are series converter and shunt converter. Series converter is regulating the voltage across sensitive load by the bus voltage. The shunt converter regulates the voltage regulation in one of the feeder. However, since the source impedance is very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance because the dc-link capacitor voltage is not regulated.

In this paper, multi converter unified power quality conditioner (MC-UPQC) is designed for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation between two adjacent feeders. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations. The performance of the MC-UPQC as well as the adopted control algorithm is illustrated by simulation. The results obtained in MATLAB/SIMULINK on a two-bus/two-feeder system show the effectiveness of the proposed configuration.

2. Proposed MC-UPQC System

A. Circuit Configuration

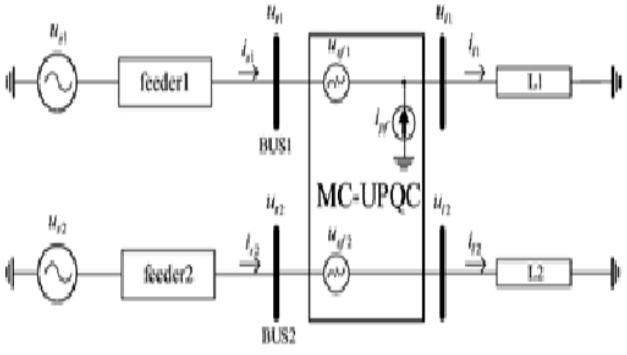

Figure 1: Single-line diagram of a distribution system with an MC-UPQC.

The fig.1 shows the single line diagram of a distribution

system with MC-UPQC, two different gene-rating stations can supply the two different loads L1 and L2 through two different feeders. The MC-UPQC is connected to two supply voltages are u_{s1} and u_{s2} through buses BUS1 and BUS2 with voltages of u_{t1} and u_{t2} respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of i_{pf} .The feeder currents are denoted by i_{s1} and i_{s2} and load currents are i_{l1} and i_{l2}.

The two Bus voltages u_{t1} and u_{t2} are subjected to distortion and sag/swell. A pure sinusoidal voltage required for nonlinear /sensitive load1, if the current has non-sinusoidal and contains harmonics. Voltage sag/swell, distortion and interruption for sensitive/critical load2 is must be fully protected and it needs pure sinusoidal voltage. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economical losses or human damages.

B. MC–UPQC Structure

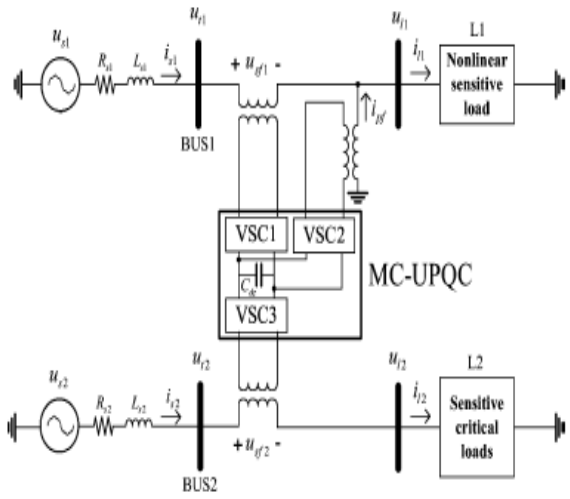

Figure 2: Typical MC-UPQC used in a distribution system.

The MC-UPQC consists of three VSCs (VSC1, VSC2, and VSC3) which are connected to a common dc-link capacitor with back to back connection. In the proposed configuration, VSC1 and VSC3 are connected in series with BUS1 and BUS2 respectively. The VSC2 is connected in parallel with load L1 at the end of Feeder1.

The each of the three VSCs in Fig. 2 is designed by commutation reactor and high pass output filter connected to a three-phase converter as shown in Fig. 3. The commutation reactor (L_f) and high pass output filter (R_f, C_f) are connected to prevent the flow of switching harmonics into the power supply.

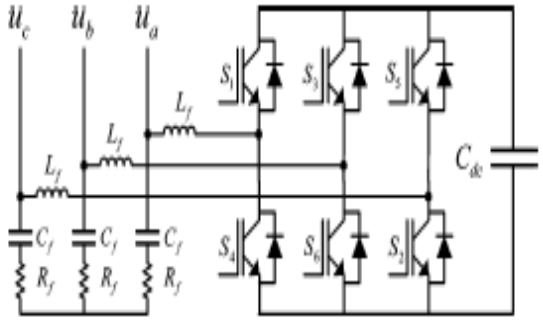

Figure 3: Schematic structure of a VSC.

As shown in Fig.2, the common dc link capacitor is supplied to all converters and these converters are connected to distribution system through transformers. The transformer primary is connected to VSCs and secondary is connected to distribution system i.e. VSC1 and VSC3 are in series with bus1, bus2 and VSC2is in parallel with load1.The objective of the MC-UPQC shown in Fig.2 are:

1) To mitigate the load voltage (u_{l1}) against sag/swell and disturbances in the system to protect the non-linear/sensitive load L1.
2) To mitigate the load voltage (u_{l2}) against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2.
3) To compensate for the reactive and harmonic components of nonlinear load current (i_{l1}).

The above objectives are achieved by operating the series VSCs as voltage controllers and shunt VSC as a current controller.

C. Control Strategy

The MC-UPQC consists of three VSCs. The switching control strategy of the two series VSCs are designed by using sinusoidal pulse width modulation (SPWM) voltage control and shunt VSC is by using SPWM hysteresis current control. Details of the control algorithm, which are based on the d-q method [6], will be discussed later.

Shunt-VSC: Functions of the shunt-VSC are:

1) To compensate for the reactive component of load1 current;
2) To compensate for the harmonic components of load1 current;
3) To regulate the voltage of the common dc-link capacitor.

Fig. 4 shows the control block diagram for the shunt VSC. The measured load current $(i_{l_abc})$is transformed into the synchronous dq0 reference frame by using $i_{l\_abc} = T_{abc}^{dq0} i_{l\_abc}$ (1)

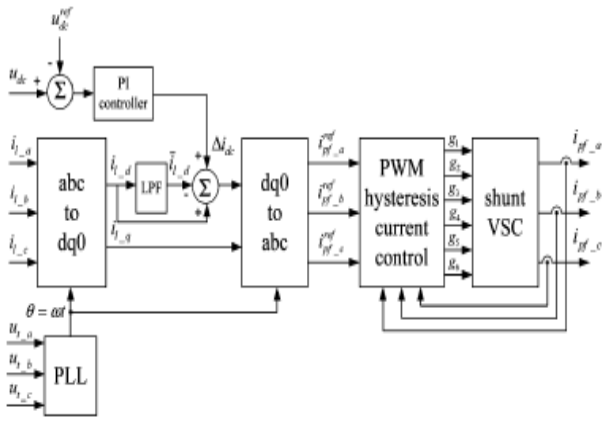

Figure 4: Control block diagram of the shunt VSC

Where the transformation matrix is

$$T_{abc}^{dqo} = \frac{2}{3}\begin{bmatrix} \cos(wt) & \cos(wt-120) & \cos(wt+120) \\ -si(wt) & -\sin(wt-120) & -\sin(wt+120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the d and q axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

$$i_{l\_d} = \bar{i}_{l\_d} + \tilde{i}_{l\_d} \quad (2)$$

$$i_{l\_q} = \bar{i}_{l\_q} + \tilde{i}_{l\_q} \quad (3)$$

Where i_{l_d}, i_{l_q} are d-q components of load are current, $\bar{i}_{l\_d}, \bar{i}_{l\_q}$ are dc components, and $\tilde{i}_{l\_d}, \tilde{i}_{l\_q}$ are the ac components of i_{l_d} and i_{l_q}. If i_s is the feeder current and i_{pf} is the shunt VSC current and knowing $i_s = i_l - i_{pf}$, then d–q components of the shunt VSC reference current are defined as follows:

$$i_{pf\_d}^{ref} = \tilde{i}_{l\_d} \quad (5)$$

$$i_{pf\_q}^{ref} = i_{l\_q} \quad (6)$$

Consequently, the d–q components of the feeder current are

$$i_{s_d} = \bar{i}_{l_d} \quad (7)$$

$$i_{s\_q} = 0 \quad (8)$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in Fig. The input of the PI controller is the error between the actual capacitor voltage (u_{dc}) and its reference value (u_{dc}^{ref}). The output of the PI controller $(i.e., \Delta i_{dc})$ is added to the d component of the shunt-VSC reference current to form a new reference current as follows:

$$i_{pf\_d}^{ref} = \tilde{i}_{l\_d} + \Delta i_{dc} \quad (9)$$

$$i_{pf\_q}^{ref} = i_{l\_q} \quad (10)$$

As shown in Fig.4, the reference currents in (9) & (10) is then transformed back into the abc reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained

$$i_{pf\_abc}^{ref} = T_{dqo}^{abc} i_{pf\_dqo}^{ref} ; \left(T_{dqo}^{abc} = T_{abc}^{dqo\,-1}\right) \quad (12)$$

Series-VSC: Functions of the series VSCs in each feeder are:
1) To mitigate voltage sag and swell;
2) To compensate for voltage distortions, such as harmonics;
3) To compensate for interruptions (in Feeder2 only).

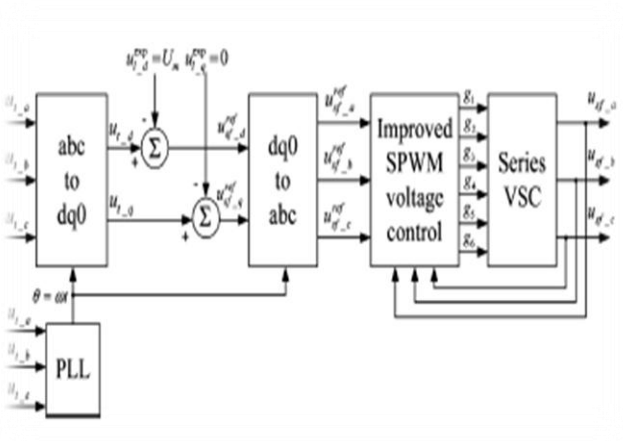

Figure 5: Control block diagram of the series VSC.

The control block diagram of each series VSC is shown in Fig.5. The bus voltage (u_{t_abc}) is detected and then transformed into the synchronous dq0 reference frame using

$$u_{t\_dqo} = T_{abc}^{dqo} u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th} \quad (13)$$

$$\begin{cases} u_{t1p} = [u_{t1pd} \quad u_{t1pq} \quad 0]^T \\ u_{t1n} = [u_{t1nd} \quad u_{t1nq} \quad 0]^T \\ u_{t10} = [0 \quad 0 \quad u_{00}]^T \\ u_{th} = [u_{th\_d} \quad u_{th\_q} \quad u_{th\_0}]^T \end{cases} \quad (14)$$

Where u_{t1p}, u_{t1n} and u_{t10} are fundamental frequency positive, negative, and zero sequence components, respectively, and u_{th} is the harmonic component of the bus voltage. According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous dq0 reference frame $\left(u_{l\_dq0}^{exp}\right)$ only has one value.

$$u_{l\_dq0}^{exp} = T_{abc}^{dq0} u_{l\_abc}^{exp} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix} \quad (15)$$

Where the load voltage in the abc reference frame $\left(u_{l\_dq0}^{exp}\right)$ is $u_{l\_abc}^{exp} = \begin{bmatrix} U_m \cos(wt) \\ U_m \cos(wt-120) \\ U_m \cos(wt+120) \end{bmatrix}$ (16)

The compensating reference voltage in the synchronous dq0 reference frame $\left(u_{sf\_dq0}^{ref}\right)$ is defined as

$$u_{sf\_dq0}^{ref} = u_{t\_dq0} - u_{l\_dq0}^{exp} \quad (17)$$

This means u_{t1p_d} in (14) should be maintained at U_m while all other unwanted components must be eliminated. The compensating reference voltage is (17) then transformed back into the abc reference frame. By using an improved

SPWM voltage control technique (sine PWM control with minor loop feedback) [8], the output compensation voltage of the series VSC can be obtained.

3. Simulation Results

The proposed MC-UPQC and its control schemes have been tested through extensive case study simulations using MATLAB/SIMULINK. In this section, simulation results are presented, and the performance of the proposed MC-UPQC system is shown.

A. Distortion and Sag/Swell on the Bus Voltage

The above system contains two three phase supply sources of 380v (rms, L-L) with 50hz.The bus1 voltage contains seventh order harmonic with a value of 22%and voltage sag of 25% between 0.1s< t <0.2s and voltage swell of 20% between 0.2s< t <0.3s.The bus2 voltage contains 35% of fifth harmonic and voltage sag of 35% between 0.15s< t <0.25s and voltage swell of 30% between 0.25s< t <0.3s.The load1 is RC load and load2 is RL load of values 10Ω and 30 μF and 10Ω and 100mH respectively.

The MC–UPQC is switched on at t=0.02s. Only the phase a waveform of BUS1 voltage, series compensating voltage and load L1 voltage are shown in Fig.4.and the BUS2 voltage, series compensating voltage and load L2 voltage are shown in Fig.5.The nonlinear load1 current, shunt compensation current, feeder1 current and dc link capacitor voltage are shown in fig.6.The MC-UPQC compensates the distorted voltages of BUS1 and BUS2 and nonlinear load current very well and the total harmonic distortion (THD) of the feeder current is reduced from 28.5% to less than 5%. Also, the dc voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders.

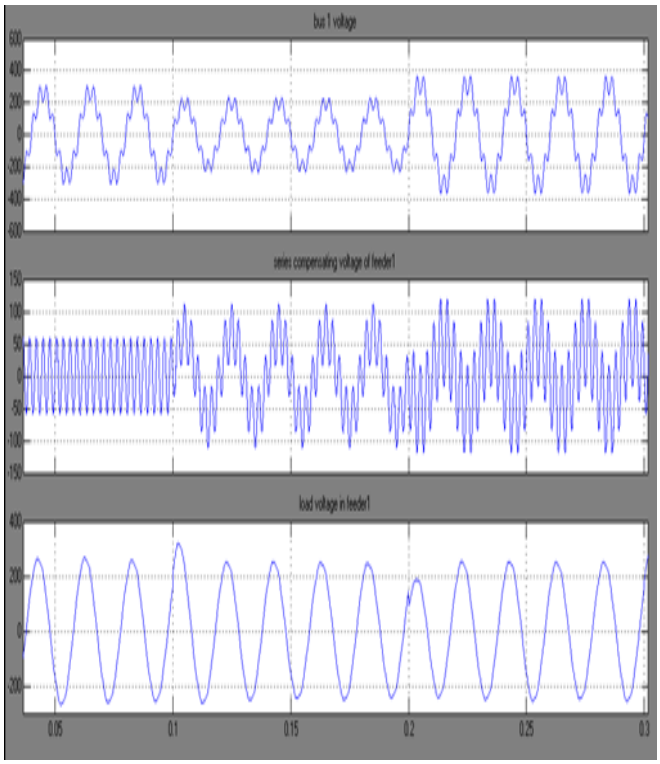

Figure 4: BUS1 voltage, series compensating voltage and load voltage in Feeder1.

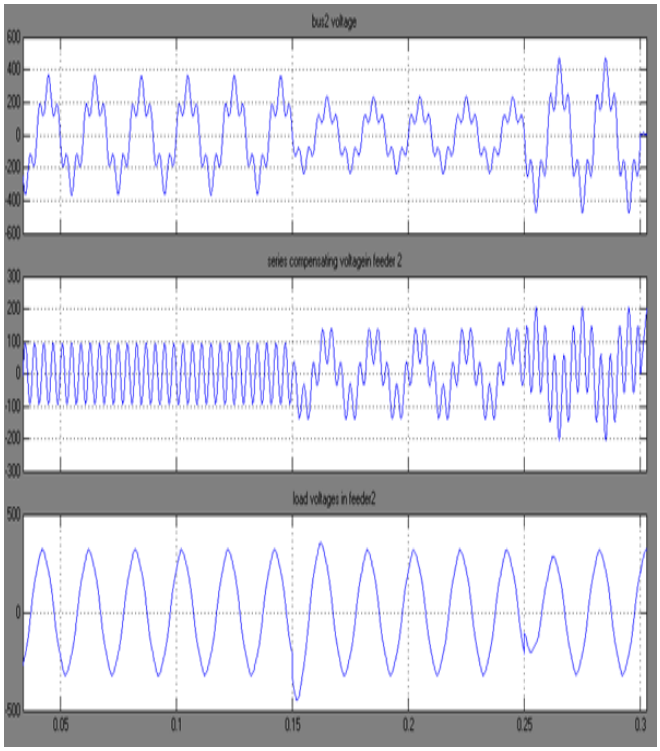

Figure 5: BUS2 voltage, series compensating voltage, and load voltage in Feeder2.

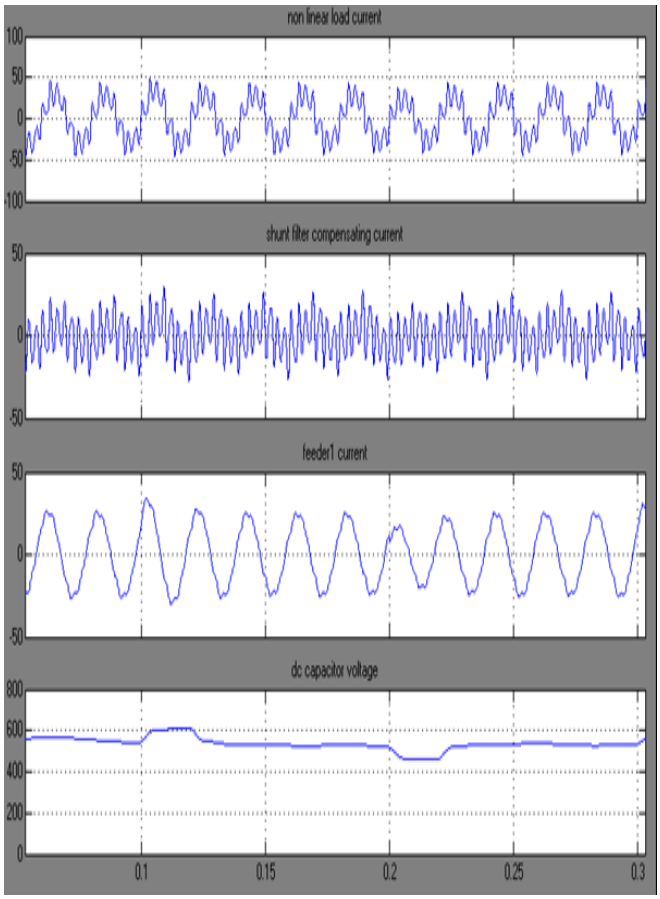

Figure 6: Nonlinear load current, compensating current, Feeder1 current, and capacitor voltage.

B. Upstream Fault on Feeder2

If there is any fault occurs in feeder2 that will cause the voltage imperfections i.e. sag/swell (or) interruption. This will be compensated by VSC2. If a tree phase to ground fault occurs at feeder2 between 0.3s< t <0.4s.Then the power

required for load2 is supplied through VSC2 and VSC3.That increases the power transfer capability of VSC2 and VSC3, this will increases cost. The cost is recovered by CAIDI and CAIFI charging higher tariffs for the protected lines for few years. The BUS2 voltage, compensating voltage and load1, load2 voltages are shown in fig.7 at three phase to ground fault condition.

C. Load Change

When the nonlinear load 1 is doubled at t=0.5s and the other load is unaltered. The load voltages of load1 and load2 are remaining undisturbed. The nonlinear load1 current, feeder1 current, load1 voltage, load2 voltage and dc-link capacitor voltage are shown in fig.8.

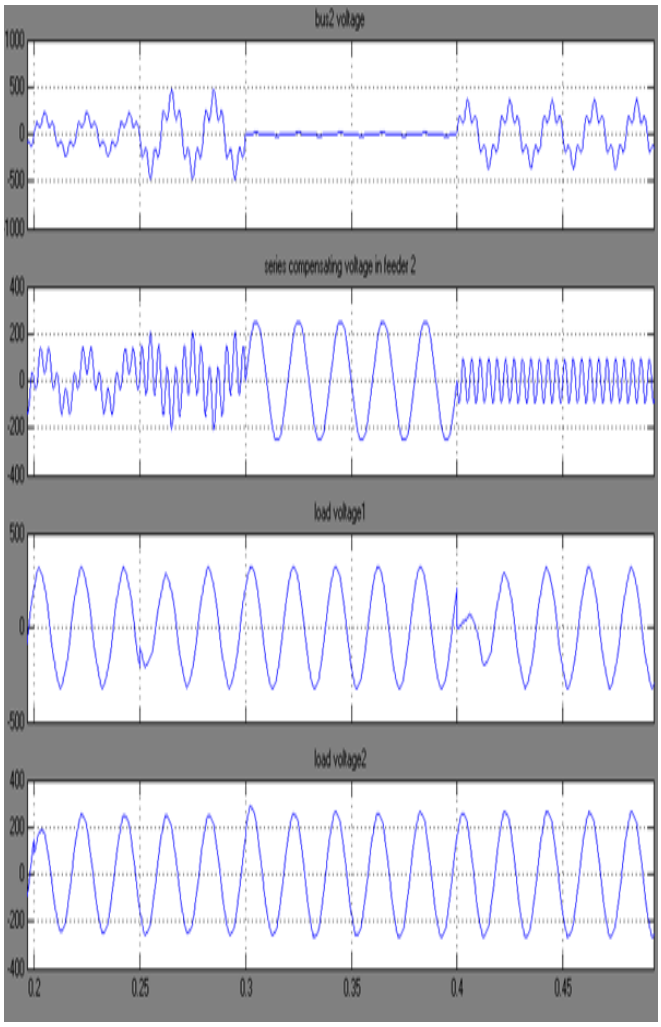

Figure 7: Simulation results for an upstream fault on Feeder2: BUS2 voltage, compensating voltage, and loads L1 and L2 voltages.

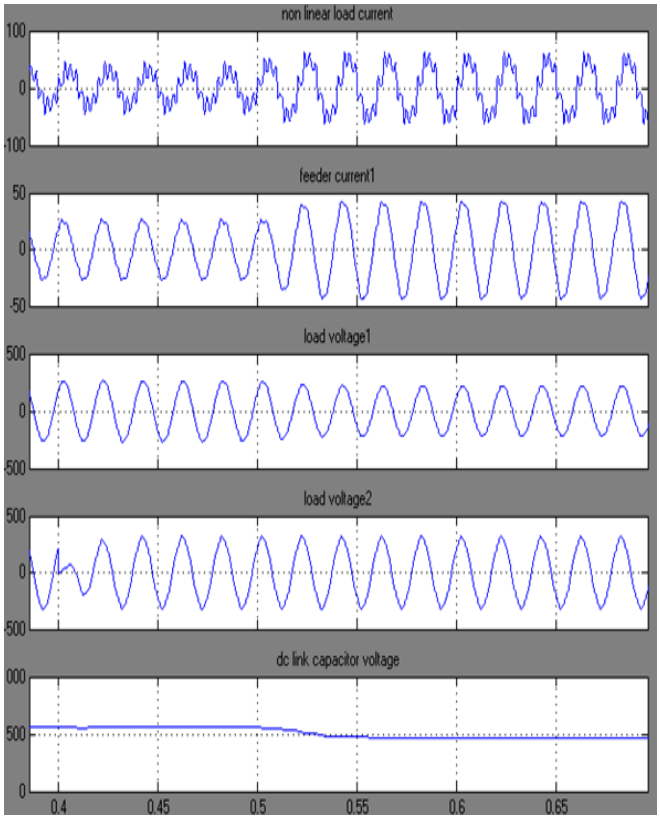

Figure 8: Simulation results for load change: nonlinear load current, Feeder1 current, load L1 voltage, load L2 voltage, and dc-link capacitor voltage.

D. Unbalance Voltage

The control strategies for shunt and series VSCs, which are introduced in Section II, are based on the d–q method. They are capable of compensating for the unbalanced source voltage and unbalanced load current. To evaluate the control system capability for unbalanced voltage compensation, a new simulation is performed. In this new simulation, the BUS2 voltage and the harmonic components of BUS1 voltage are similar to those given in Section IV. However, the fundamental component of the BUS1 voltage $\left(U_{t1,fundamental}\right)$ is an unbalanced three-phase voltage with an unbalance factor $\left(\frac{U_-}{U_+}\right)$ of 40%. This unbalance voltage is given by

$$\left(U_{t1,fundamental}\right) = \begin{bmatrix} 0.31\cos(wt + 44) \\ 0.31\cos(wt - 106) \\ 0.155\cos(wt - 210) \end{bmatrix}$$

The simulation results for the three-phase BUS1 voltage, series compensation voltage and load voltage in feeder 1 are shown in Fig.9. The simulation results show that the harmonic components and unbalance of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

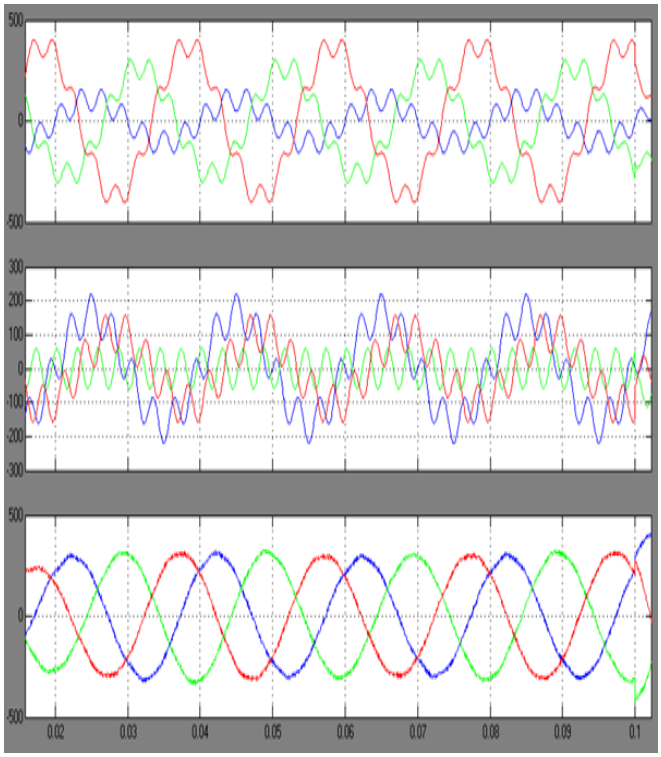

Figure 9: BUS1 voltage, series compensating voltage, and load voltage in Feeder1 under unbalanced source voltage.

4. Conclusion

In this paper, the multi converter unified power quality conditioner is designed for simultaneous compensa-tion of voltage and current imperfections in adjacent feeders. This topology is fully protected critical and sensitive loads against distortions, sag/swell and interruption in two feeder system. The MC-UPQC has power transfer between two adjacent feeders for sag/swell and interruption compensation without need of battery storage. The idea can be extended to multi bus/multi feeder system by adding more series VSCs for various disturbance conditions.

References

[1] Hamid Reza Mohammadi, Ali Yazdian Varjani, and Hossein Mokhtari, "Multiconverter Unified Power-Quality Conditioning System: MC- UPQC" IEEE RANSACTIONS ON POWER DELIVERY, VOL.24,NO. 3, JULY 2009.

[2] H. Akagi, "New trends in active filters for power conditioning," *IEEETrans. Ind. Appl.*, vol. 32, no. 6, pp. 1312–1322, Nov./Dec. 1996.

[3] M. Rastogi, R. Naik, and N. Mohan, "A comparative evaluation of harmonic reduction techniques in three-phase utility interface of power electronic loads," *IEEE Trans. Ind. Appl.*, vol. 30, no. 5, pp. 1149–1155,Sep./Oct. 1994.

[4] F. Z. Peng, "Application issues of active power filters," *IEEE Ind. Appl Mag.*, vol. 4, no. 5, pp. 21–30, Sep../Oct. 1998.

[5] L. Gyugyi, K. K. Sen, and C. D. Schauder, "Interline power flow controller concept: A new approach to power flow management in transmission systems," *IEEE Trans. Power Del.*, vol. 14, no. 3,pp.1115–1123, Jul. 1999.

[6] B. Fardanesh, B. Shperling, E. Uzunovic, and S. Zelingher, "Multi-converter FACTS Devices: The generalized unified power flow controller (GUPFC)," in *Proc. IEEE Power Eng. Soc. Summer Meeting*,2000, vol. 4, pp. 2511–2517.

[7] M. Hu and H. Chen, "Modeling and controlling of unified power qualitycompensator," in *Proc. 5th Int. Conf. Advances in PowerSystem Control, Operation and Management*, Hong Kong, China,2000, pp.431–435.

Author Profile

Mr. D.Subba Rao received the B.Tech degree in Electrical and Electronics Engineering from JNTU University, Hyderabad, India in 2008, and the M.Tech degree in Power Systems Engineering from Acharya Nagarjuna University, India in 2012.He is currently working as Assistant Professor in the department of Electrical and Electronics Engineering at KKR & KSR Institute of Technology and Sciences, Guntur Dist., Andhra Pradesh, India. His research areas include Power Systems and Power Quality

Mr. T.Srinivasa Rao was born in 1961. He received B.Tech degree in Electrical and Electronics Engineering from college of Engineering, Kakinada in 1982 and M.E degree in Control Systems from PSG College of Technology, Coimbatore, India in 1985. Currently he is working as Professor and HOD EEE Department at KITS, Guntur. His research interests include Control systems, Robotics, Embedded Systems, Power Systems and Power Quality.