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Simulation of Silicon Nanowire Field Effect Transistor for Different High k Dielectric Material

Prabhat Shukla[1], Swapnali Makdey[2]

[1]M.E. Electronics Engineering, Fr. Conceicao Rodrigues College of Engineering, Mumbai University
Bandstand-Bandra (W), Mumbai, India

[2]Professor, M.E. Electronics Engineering, Fr. Conceicao Rodrigues College of Engineering, Mumbai University
Bandstand-Bandra (W), Mumbai, India

Abstract: ***Scaling of the MOSFET leads to the better performance of the device up to certain extent but further scaling when channel length approaches from µm to nm regime leads to short channel effects such as subthreshold voltage, drain induced barrier lowering etc. This paper discuss about the simulation of Silicon Nanowire Field Effect with different high –k dielectric material such as SiO2, ZrO2 and HfO2 at different temperature for different gate control parameter. By keeping diameter and gate insulation thickness constant we conclude that as we go for high – k dielectric material there is better response for On current, leakage current and quantum capacitance limit..***

Keywords: Leakage current, threshold voltage, Ballistic transport, silicon Nanowire transistor and Quantum capacitance limit

1. Introduction

The large amount of research is going on to enhance the performance of the electronic device. The device scaling has successfully predicted by the Moore's Law 0[2]-the number of transistors on one IC chip has quadrupled every three years and the feature size has shrunk to half of its original value at the same time. Scaling of the MOSFET gave a significant response to the input given to it but as channel length varies from µm to nm regime Short Channel Effect (SCE) exists in the device such as subthreshold voltage, leakage current, drain induced barrier lowering (DIBL) etc. to overcome this new device has to be investigated. In Double gate MOSFET gate control doubled but as L/W ratio becomes greater than 2, this invests the problem of lithography and again a new transistor design is sought [3]. Silicon Nanowire Field Effect Transistor (SiNWFET) is perceived to be future device which will replace the MOSFET. In SiNWFET gate is all around the channel, therefore the current flow can be controlled very well. This ensures less power consumption and hence more efficiency. To gate the better response SiNWFET is operated at ballistic transport [4] and within quantum confinement limit. Silicon Nanowire is compatible with the current CMOS process. In this paper we have used SiNWFET with different gate oxide material such as SiO2, ZrO2 and HfO2 to study the drain current vs gate voltage, drain voltage and quantum capacitance vs gate voltage. The tool used for the simulation is fettoy tool available on the nanohub.org [5].

2. Silicon Nanowire Field Effect Transistor

In simple SiNWFET the transconductance and electron mobility is found less and this was due to the bad contacts of silicon Nanowire at source and drain junctions but this was improved with the help of thermal annealing and passivation of oxide defects by chemical modifications were found to increase the average transconductance from 45 to 800 nS & average mobility from 30 to 560 cm2/V.sec with peak values from 2000 nS & 1350 cm2/V.sec [6]. This improved source drain contact with silicon Nanowire lithography becomes simple. As mobility and transconductance of the device is improved this in turn increases the voltage gain of the device. As compared to MOSFET, SiNWFET has better gate control, as gate is all around the channel and hence has better control of drain current. Due to scaling of the device, to maintain the gate oxide capacitance the gate oxide thickness reduces and leakage current becomes prevalent. Conventional gate oxide used is SiO2 (k = 3.9), by increasing dielectric constant of the gate oxide material such as ZrO2 (k = 15) and HfO2 (k = 25) reduction in the thickness is maintained constant as gate capacitance is compensated by increase in the dielectric constant k & due to this leakage current is reduced up to its minimum value. SiNWFET is operated at Ballistic transport, by operating so scattering of electron is avoided. Channel length scaling of Silicon Nanowire field effect transistor can be done and current voltage characteristics is obtained by self consistently solving the Non Equilibrium Gate function (NEGF) transport equation with Poisson's equation [7]. SiNWFET follows Poisson's equation [8] and the same is modelled by it. The equation is solved by obtaining various parameters

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r.\frac{\partial}{\partial r}\varnothing_i(r,z)\right)+\frac{\partial^2}{\partial z^2}\varnothing_i(r,z)=\frac{-qN_D}{\epsilon_j}$$

Where r is the radial distance, z is the position along the channel, $\varnothing_i$(r, z) is the potential of the material depending on the radius & position along the channel, N_D is the doping concentration. Total potential is zero at the centre of the silicon Nanowire field effect transistor and it is maximum at the boundaries called surface potential.

The SiNWFET is operated in the quantum confinement limit so as to get the better result [9]. For improving the device performance different high dielectric material is used

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[10],[11]. SiNWFET is also simulated for different gate control parameter. Gate control parameter is defined as ratio of gate capacitance to sum of gate, source and drain capacitance. Drain control parameter is kept constant at 0.035 [12].

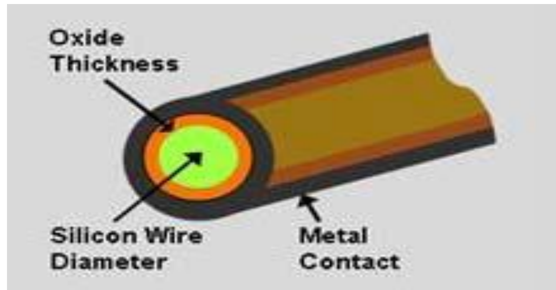

Figure 1: Structure of silicon Nanowire transistors with oxide thickness and metal contact [5]

3. Simulation Result and Discussion

In this paper we have simulated SiNWFET at ballistic transport within quantum confinement limit. Here tool used is fettoy available on the nanohub.org [5]. Here we have kept silicon Nanowire diameter and gate oxide thickness at 5 nm and valley degeneracy is 2. The input parameters are as given in the below table:

Table 1: Input Parameters

Parameter	Value
SiNWFET Diameter	5nm
Gate Insulation thickness	5nm
Valley degeneracy	2
Drain Control Parameter	0.035
Threshold Voltage	0.2 V

After simulation we have observed the below characteristics for different high k dielectric materials and their respective explanation is also mentioned in that.

3.1 Drain Current Vs Gate Voltage at GCP=0.92, T=300K

There exist high leakage current in case of SiO2 but as the dielectric constant of the material increases, the leakage current of the device vanishes or can be said to be greatly reduced because as gate voltage increases the oxide thickness decreases in case of material with low dielectric constant but it remains almost unaffected as high k dielectric material is used

As dielectric constant k increases the threshold voltage is decreases and due to this leakage current is reduced.

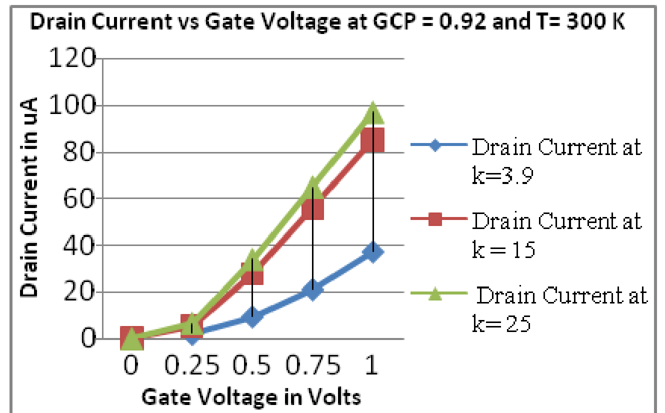

Figure 2: Drain current vs Gate voltage

3.2 Drain Current Vs Drain Voltage at GCP=0.92, T=300K

For higher gate voltages as the dielectric constant of the material increases it gives favourable response by having higher drain current than in the conventional SiO2 as its gate oxide material. This would enable the device to lower the DIBL. High k dielectric curve saturate at higher drain current and hence the drive current increases.

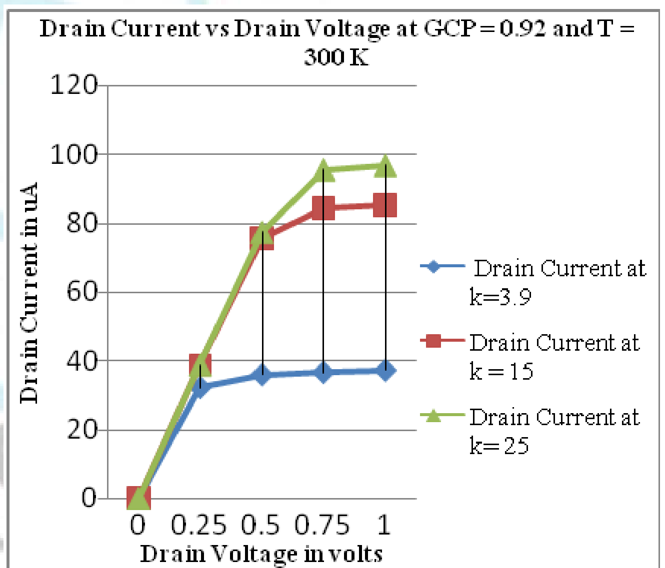

Figure 3: Drain Current vs Drain Voltage

3.3 Quantum Capacitance Vs Gate Voltage aT GCP=0.92, T=300K

A device is said to be in quantum capacitance limit when gate capacitance is greater than quantum capacitance. Device is operated near to quantum confinement limit when quantum capacitance is lower at high voltage than low gate voltage. We can see from the characteristic diagram of quantum capacitance to gate voltage that as dielectric constant of the material increases the value of quantum capacitance decreases at higher gate voltage. Therefore from the above characteristic we can conclude that as dielectric constant of the gate oxide material increases SiNWFET is more near to quantum confinement limit.

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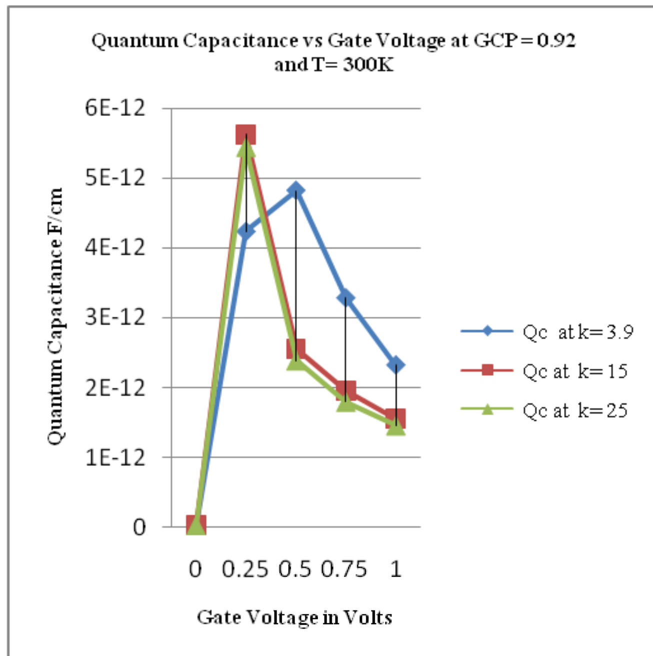

Figure 4: Quantum Capacitance vs Gate Voltage

4. Conclusions

SiNWFET with keeping diameter and gate insulation thickness constant at 5nm, and under the ballistic transport condition results obtained on simulator shows the better response for On current, leakage current and quantum capacitance limit for high –k dielectric material such as Zirconium dioxide and HfO2 as compared to conventional SiO2.

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Author Profile

Prabhat Shukla received the B.E. degrees in Electronics and Tele Communication Engineering from Konkan Gyanpeeth College of Engineering, Karjat in 2011. Presently pursuing M.E. in Electronics Engineering from Fr. Conceicao Rodrigues College of Engineering Bandra, Mumbai
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