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Implementation of Logic Gates using the Dual Mode Logic and their Applications

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Abstract: ***In this paper, a Johnson up-counter was designed by using the different types of flip flops. Here the D-flip flop was designed using the DML type_A NAND gate, and TSPC D-flip flop using the DML(Dual Mode logic) logic in order to reduce the power dissipation. The TSPC_DML flip flop has less power compared to the D-flip flop. The Dual Mode Logic (DML) family provides a novel approach to providing this capability by introducing two configurable operating modes, static and dynamic. The dual mode logic gates has very low-power dissipation with moderate performance in the static mode of operation. The proposed TSPC D- flip-flop in which the number of transistors are reduced from 11 transistors to 5 transistors. As number of transistors are reduced in occupies less area and also the power will be reduced compared to the conventional TSPC (True ingle phase clock)D- flip-flop.***

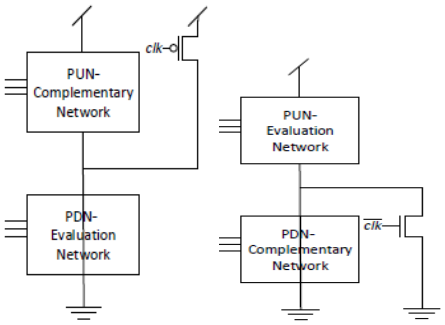
Keywords: Basic gates, D- Flip flop, TSPC-D Flip flop, Johnson counter.

1. Introduction

Now-a-days in the VLSI design, the major concern is low-power high speed and area efficient circuit design. For the manufacturers the ultra low-power circuit design has become a key design in maximum number of applications. When compared to performance and speed the power reduction is the highest factor due to some technological advancements. In this paper, the low-power design of 4-bit up Johnson counter has been proposed by using TSPC(True single phase clock) circuit which has been designed using DML(Dual mode logic).

2. Dual Mode Logic

For the high-performance applications the dynamic logic which is termed as domino logic has been widely used. Many attempts to domino logic has been failed due to the high sensitivity to process variations in nano-scale technologies. Now, a novel logic family has been introduced termed as Dual Mode Logic(DML) which operates in sub-threshold region. Here, the proposed logic can be two modes one is the static CMOS like mode and the other is the dynamic np-CMOS-like mode. With the moderate performance the dual mode gate has very low power dissipation in the static mode of operation, while in the dynamic mode of operation the dual mode gate attain a higher performance, though with huge power dissipation. The DML has two basic topologies one is the Type_A topology and the other is the Tpye_B topology these are reffered as unfooted DML(Dual Mode Logic) gates.



(a) type_A unfooted DML (b) type_B unfooted DML

In fig.1(a) the PMOS transistor is connected at the output of the gate. By enabling the clock(clk) input the output changes. When the clock(clk) input is low the pmos transistor connected at the output conducts and then the output is precharged to Vdd. The output depends on the logic of CMOS gate when the clock (clk) input is high i.e., logic 1. In fig.1(b) the NMOS transistor is connected at the output and the drain terminal of nmos transistor is connected to ground in the Type_B topology. In this type_B topology the output depends on the standard CMOS gate when the clock (clk) input is low. When the clock input is high the NMOS transistor conducts so that the output is precharged to ground (GND). The extension to this basic DML topologies is the footed DML topology. These are referred to as Type_A footed DML gate and Type_B DML gate.

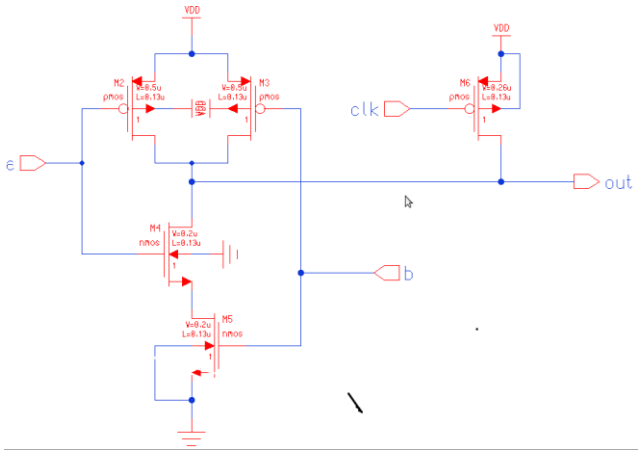


Figure 1: Schematic diagram of DML typeA NAND gate

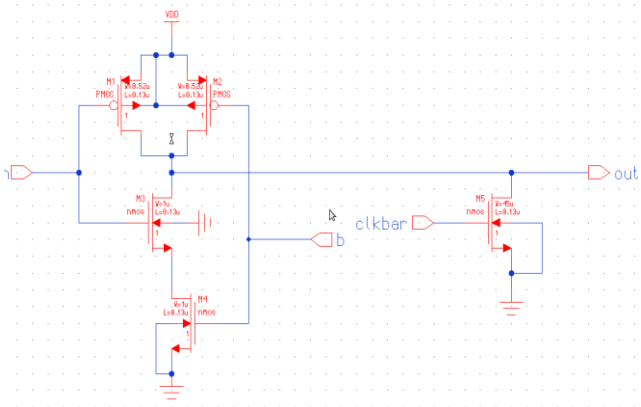


Figure 2: Schematic diagram of DML typeB NAND gate

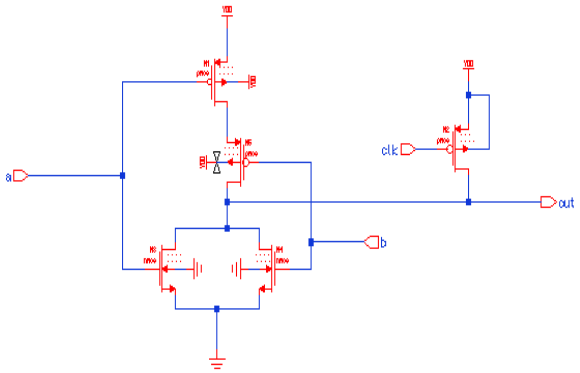


Figure 3: Schematic diagram of DML typeA NAND gate

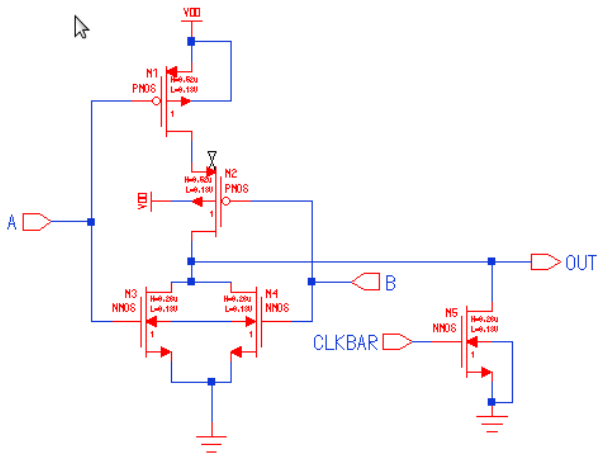


Figure 4: Schematic diagram of DML typeA NAND gate

Table 1: Comparison of power dissipation

Type of Gates	Power Dissipation
NAND GATE TYPE_A DML	386.3p watts
NAND GATE TYPE_B DML	12.16n watts
NOR GATE TYPE_A DML	7.59n watts
NOR GATE TYPE_B DML	140.6uwatts

3. Simulation Results

D-flip flop

The D-flip flop operation depends on the clock signal. When the clock(clk) signal is high then the input data appears at the output. For example when clk= high and d = high then the output Q will be 1 and when clk is low then there will be no change in the output i.e the output follows the previous data.

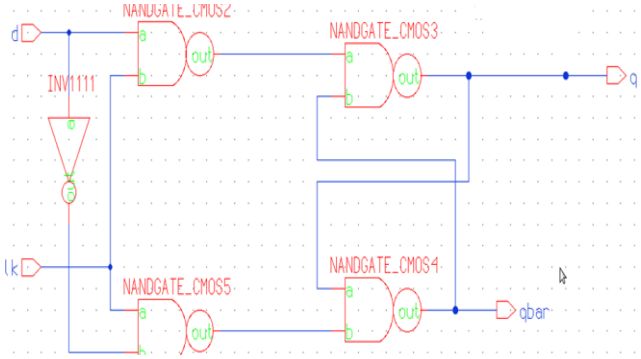


Figure 5: Schematic diagram of DML typeA NAND gate

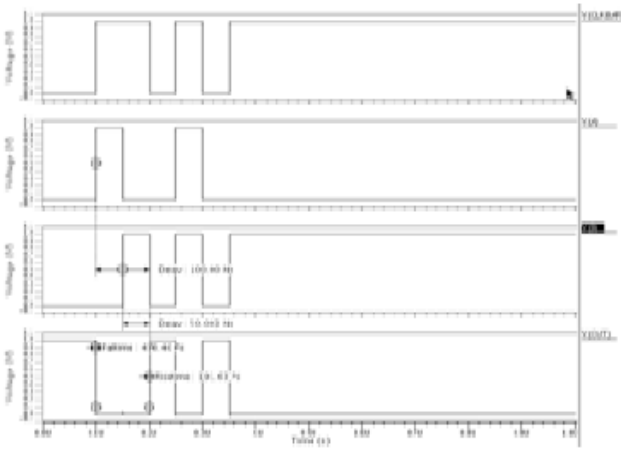


Figure 6: Simulated waveforms of DML typeA NAND gate

D-flip flop using DML NAND gate

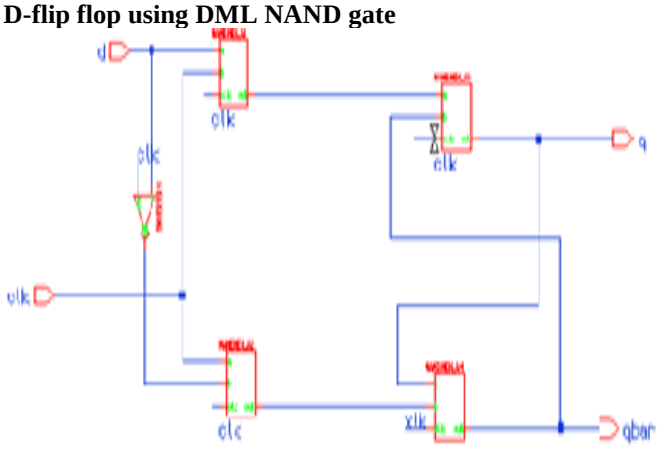


Figure 7: Schematic diagram of D-flip flop typeA DML NAND gate

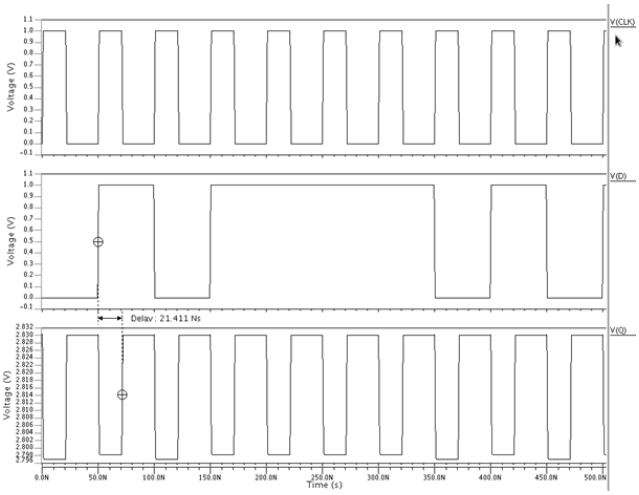


Figure 8: Simulated waveforms of D-flip flop DML typeA NAND gate

True single phase clock(TSPC) flip flop:

D-flip flop is used in designing of the TSPC(true single phase clock) flip flop. This TSPC flip flop circuit design consists of some alternating stages which are called as p-blocks and n-blocks. These blocks are driven by the same clock signal. As this TSPC flip flop design consists of D-flip flop, the operation of this TSPC circuit is same as the D-flip flop operation. In this depending on the clock signal the output changes.

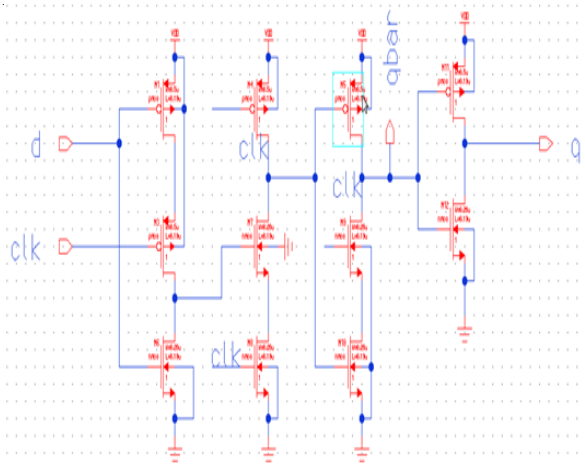


Figure 9: Schematic diagram of TSPC D-Flip flop using typeA NAND gate

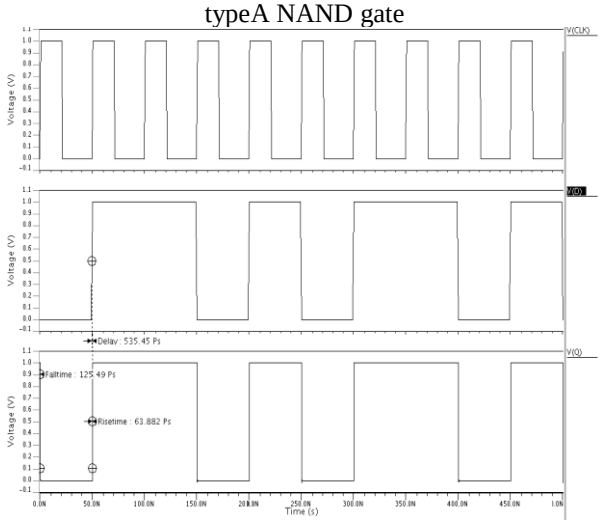


Figure 10: Simulated waveforms of TSPC- D flip flop

TSPC-flip flop using DML type_A topology:

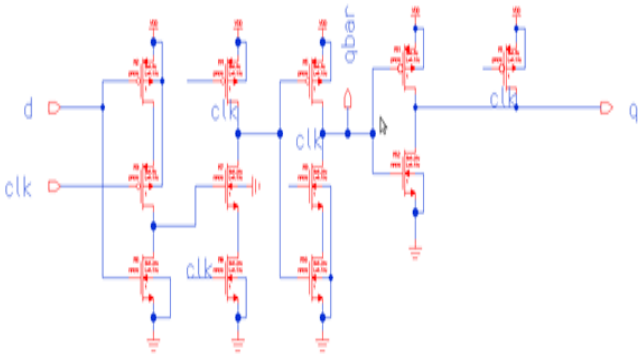


Figure 11: Schematic diagram of TSPC D-Flip flop using typeA DML gate

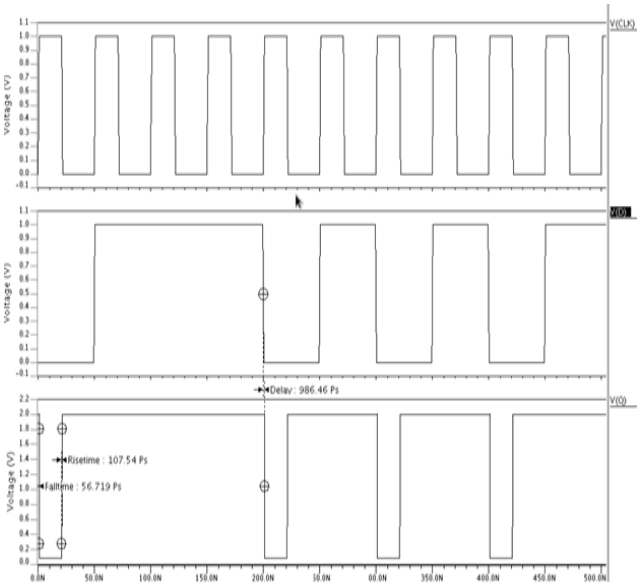


Figure 12: Simulated waveforms of TSPC D-flip flop DML typeA gate

4. Proposed TSPC flip flop

In this proposed TSPC flip flop circuit number of transistors are reduced from the conventional circuit. In this number of transistors used are five. By using this 5T-TSPC flip flop circuit the power dissipation can be reduced.

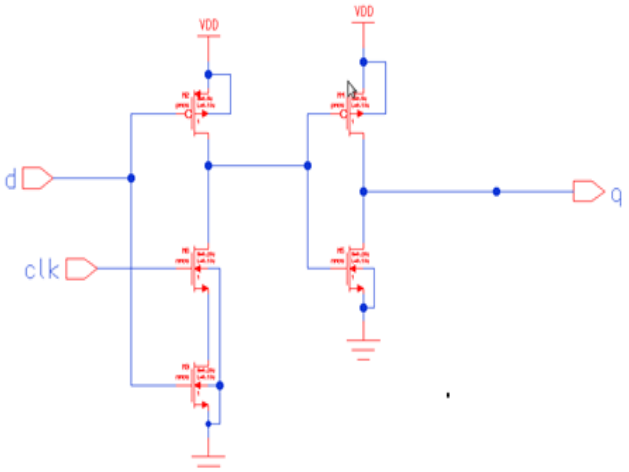


Figure 13: Schematic diagram of proposed TSPC D-Flip flop

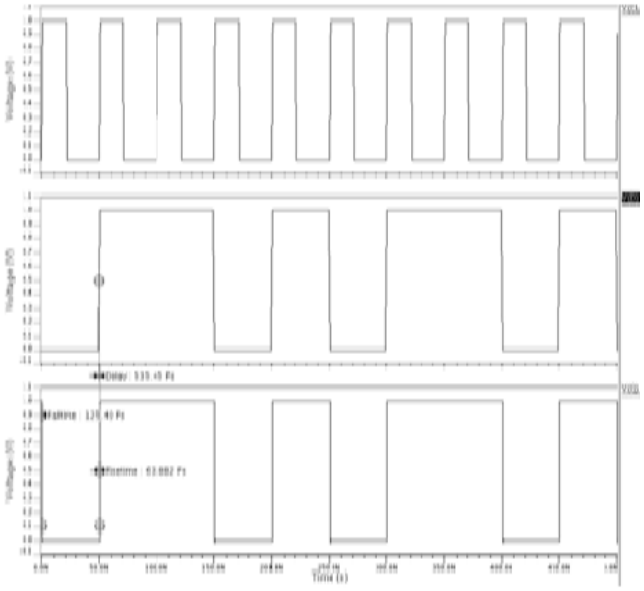


Figure 14: Simulated waveforms of proposed TSPC D-flip flop

PROPOSED 5T TSPC-FLIP FLOP USING DML:

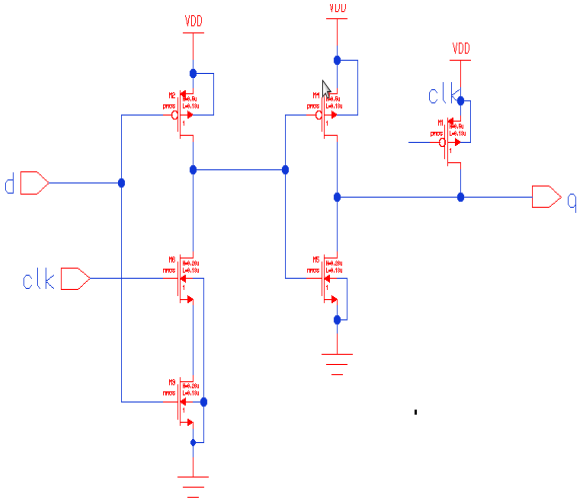


Figure 15: Schematic diagram of proposed TSPC D-Flip flop using DML typeA GATE

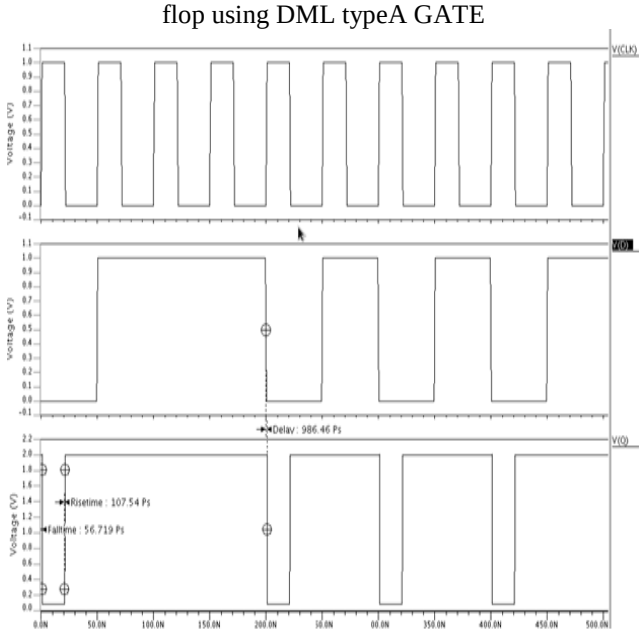


Figure 16: Simulated waveforms of proposed TSPC D-flip flop using DML typeA gate

5. Application of Flip Flops

Johnson counter using D-flip flop

In this 4-bit Johnson counter is designed. For the design of 4-bit Johnson up counter 4 stages of flip flops are used. As this Johnson counter is design using D-flip flop in this four D-flip flop stages are taken. In this clock signal is used as the input and each flip flop has two outputs one is true value output and the other is the complementary output. In this the output of one stage is connected to the next stage d-input. The complementary output of last stage is connected as feedback to the d-input of the first stage. This performs the shift register operation. This is also known as the twisted ring counter.

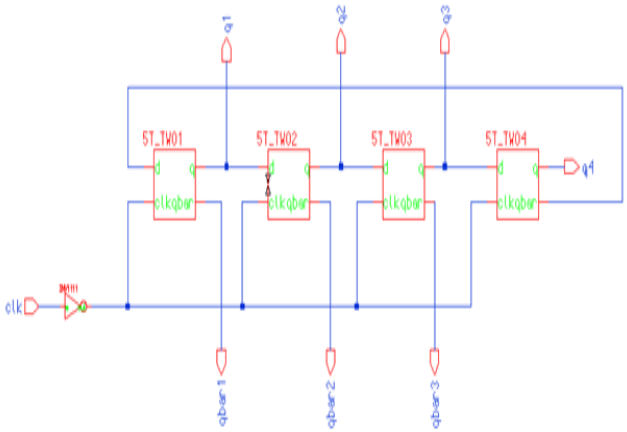


Figure 17: Schematic diagram of Johnson counter using D-Flip flop

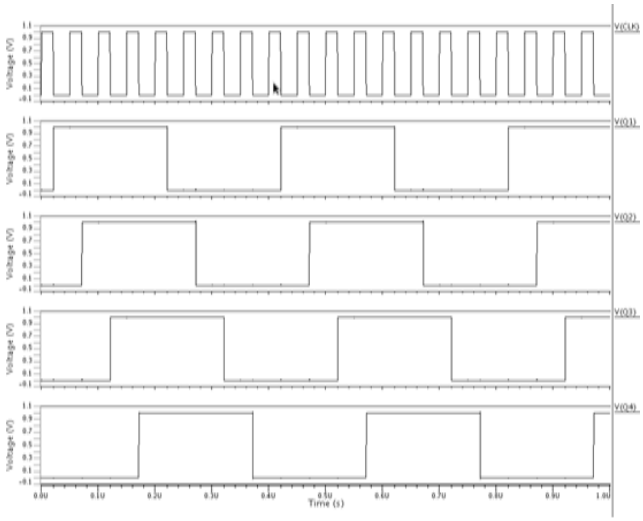


Figure 18: Simulated waveforms of johnson counter using D-flip flop

JOHNSON COUNTER USING DML:

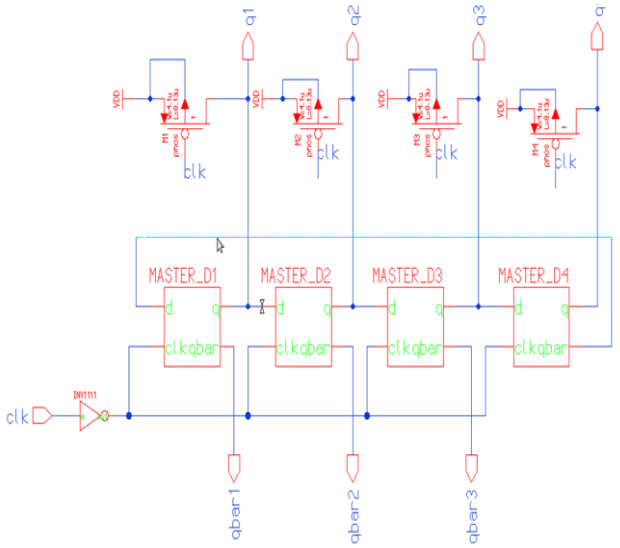


Figure 19: Schematic diagram of Johnson counter using DML D-Flip flop

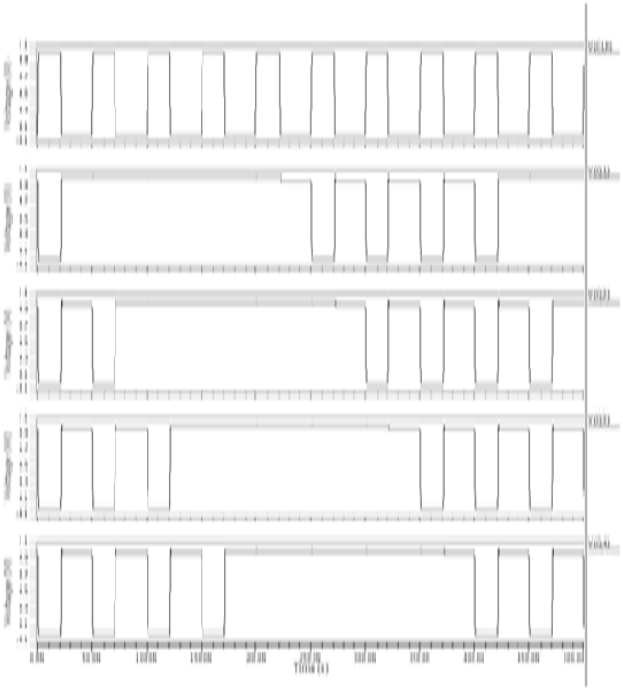


Figure 20: Simulated waveforms of Johnson counter using DML D-flip flop

JOHNSON COUNTER USING TSPC FLIP FLOP:

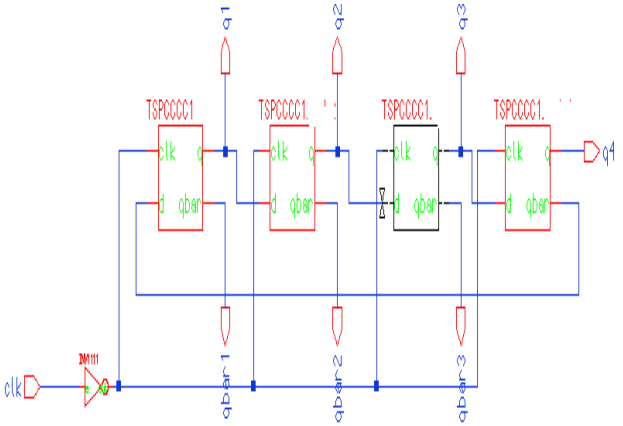


Figure 21: Schematic diagram of Johnson counter using TSPC D-Flip flop

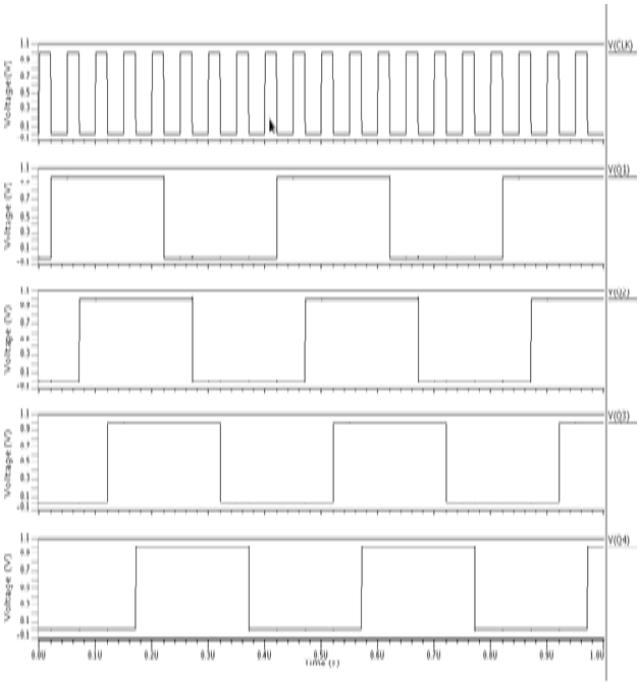


Figure 22: Simulated waveforms of johnson counter using TSPC D-flip flop

JOHNSON COUNTER USING DML TSPC FLIP FLOP:

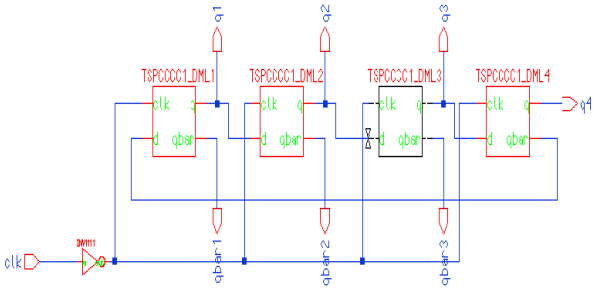


Figure 23: Schematic diagram of Johnson counter using TSPC D-Flip flop

JOHNSON COUNTER USING PROPOSED 5T- TSPC FLIP FLOP:

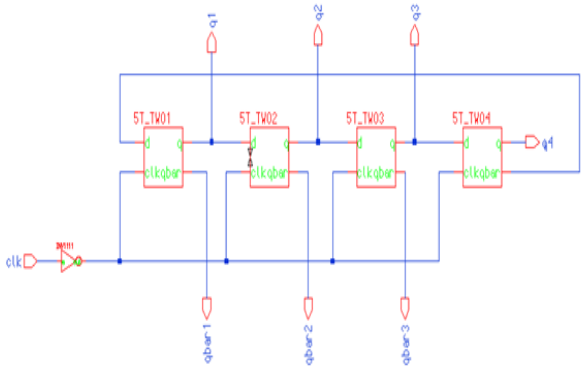


Figure 24: Schematic diagram of Johnson counter using PROPOSED 5-T DML TSPC D-Flip flop

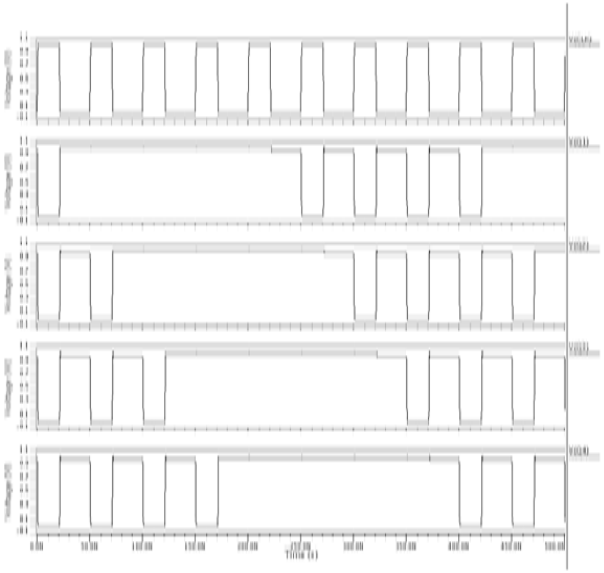


Figure 23: Schematic diagram of Johnson counter using Proposed 5-TDML TSPC D-Flip flop

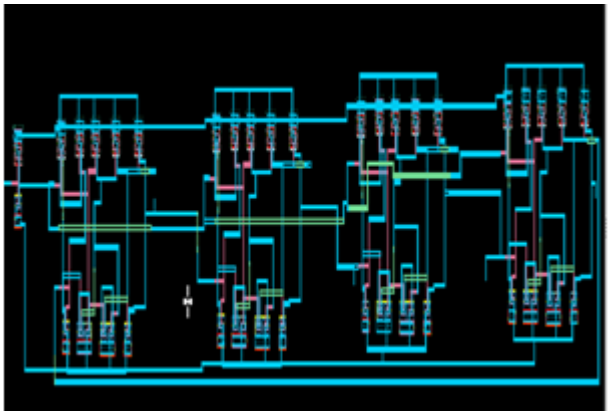


Figure 24: LAYOUT for proposed Johnson counter using DML 5-T TSPC D-Flip flop

6. Experimental Results

Table 2: Performance comparison of flip flops:

Flip-flops	Without DML	With DML
D-flip flop	17.652NWATTS	11.46NWATTS
TSPC 11T flip-flop	12.378NWATTS	9.65NWATTS
TSPC 5T Flip-flop	5.2096NWATTS	2.306NWATTS

Table 3: Power dissipation of counters

Counters	Without DML	With DML
D-flip flop	13.01mwatts	11.01mwatts
Using TSPC 11-T flip flop	6.605nwatts	4.78nwatts
Using TSPC 5-T flip flop	2.2709nwatts	1.3671nwatts

7. Conclusions

This paper proposes a low power 4-bit Johnson up- counter. The counter has been designed using the TSPC flip flop. In this in order to reduce the power dissipation the number of transistors are reduced to five. This counter was designed using 130nm technology in mentor graphics tool. As the number of transistors are reduced from 11 transistors to 5 transistors TSPC flip-flop it occupies less area and the power dissipation has been almost reduced to half of the conventional flip flop.

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