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Design of Shift Register using Pulsed Latches to Reduce Area and Power Dissipation

Lakshmi Chinnammalu R[1], V. N. Lakshmana Kumar[2]

[1, 2]Department of Electronics and Communication Engineering, MVGR College of Engineering (Autonomous), Vizianagaram, Andhra Pradesh-535005, India

Abstract: ***This paper proposes the method to design shift register using TSPC pulsed latches and clock generator circuit with GDI AND gate and one delay cell. The proposed method reduces area and power dissipation by using 130nm Mentor Graphics tool. Here, the proposed method is compared with the two conventional methods of shift registers. In one of the conventional methods, shift register is designed by using PPCFF (Power-PC style flip-flop).The flip-flop based shift register requires one clock signal for each flip-flop for its operation. In the second method, the shift register is designed by using SSASPL (Static Differential Sense Amplifier pulsed latch) and clock generator circuit with simple AND gate and some delay cells. For the operation of pulsed latch, a pulsed clock signal (a part of clock signal) is sufficient.***

Keywords: Pulsed latch, Pulsed clock, flip- flop, area, power dissipation, shift register

1. Introduction

One of the basic building blocks of VLSI circuit is the shift register. These are widely used in many applications like digital filters [2], communication receivers [3], and image processing [4]-[6].A 4K-bit shift register is used in image-extraction and vector generation VLSI chips [4].A 2K-bit shift register is used in a 10-bit 208 channel output LCD column driver IC [5].A 45K-bit shift register is used in a 16-mega-pixel CMOS image sensor [6].

To design N-bit shift register with flip-flops or pulsed latches, they are to be connected in series. To reduce area, shift register with less number of transistors is to be selected. Among different types of flip-flops and pulsed latches, the proposed TSPC pulsed latch has less number of transistors. So, the proposed shift register reduces area [7]-[10]. Power dissipation of the proposed shift register also reduces due to the use of TSPC pulsed latch and GDI clock generator circuit which contain GDI AND gate and also less number of delay cells. In this paper, proposed shift register is compared with two conventional methods of shift registers designed using PPCFF and SSASPL in terms of area and power dissipation and the design of shift register for low area and power dissipation is done by using 130nm Mentor Graphics Tool. The proposed shift register is formed by TSPC pulsed latches and a clock generator circuit to generate pulsed clock signals.

2. Conventional method 1 Shift register using PPCFF

The conventional method 1 shift register is designed using PPCFF as shown in Fig.1.One complete clock signal is used by the flip-flop for its operation [11]. The number of flip-flops required for N bit shift register are also N. The number of transistors in PPCFF are 16.The shift register using PPCFF dissipates more power and occupies more area due to more number of transistors and using complete clock cycle.

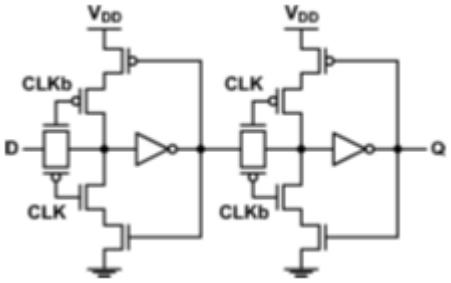

Figure 1: Conventional method1Master-Slave Flip-flop

3. Conventional method 2 Shift register using SSASPL

The architecture of conventional method 2 shift register of N bits using SSASPL is divided into sub shift registers as shown in Fig.2. Each sub shift register consists of five pulsed latches. The output of shift register is taken from first four latches and the last latch acts as temporary latch. So, for designing N bit shift register, it requires N+1 pulsed latches. Five Pulsed latches are enabled by the five non overlapping clock pulses of the clock generator circuit. These five pulsed clock signals are sufficient to design any length of shift register. The clock pulses are applied in the reverse order of the latches in the shift register. So, the updating of data is also in the reverse order of latches. Though the power dissipation of the clock generator is more, it is not taken into consideration because, the same circuit is used to design any bit shift register. Pulsed latch requires only a part of clock signal for its operation. The clock generator circuit used in Conventional method2 shift register consists of five delay cells and a basic AND gate to generate one pulsed clock signal. The generated clock signals has some more delay than it's previous.

The SSASPL as shown in Fig.3 has seven transistors [7] which are less than PPCFF with clock generation circuit to reduce area and power dissipation.

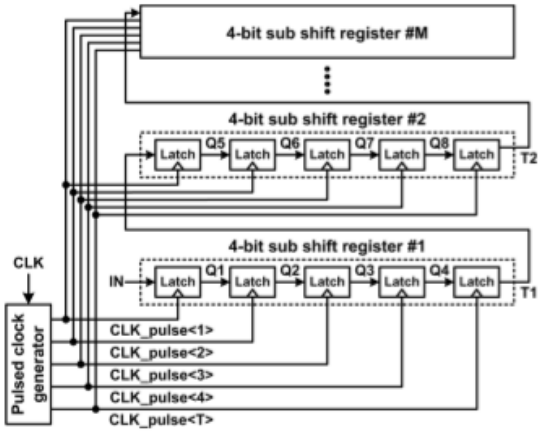

Figure 2: Conventional method 2 shift register using SSASPL

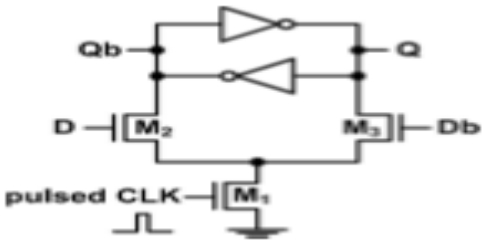

Figure 3: Schematic of SSASPL

4. Proposed Shift register using TSPC Pulsed latch

The architecture of proposed shift register using TSPC pulsed latch as shown in Fig.4 is same as conventional shift register using SSASPL. The shift register using TSPC pulsed latch also requires clock generator circuit.The number of transistors in this latch is reduced to 6 and the clock generator circuit used in this proposed shift register has less number of delay cells and GDI AND gate [17].So that the area and power dissipation is almost reduced to half of the conventional shift register designed with SSASPL.

When clock is high, the clock pulses are generated and the latch is in transparent mode and corresponds to two cascaded inverters; the latch is non-inverting and propagates input to the output. When clock is low, both the inverters are in hold mode, only the pull up networks are active and pull-down networks are deactivated. As a result no signal can propagate from input of the latch to the output in this mode. The main advantage of this proposed latch is use of single phase clock.

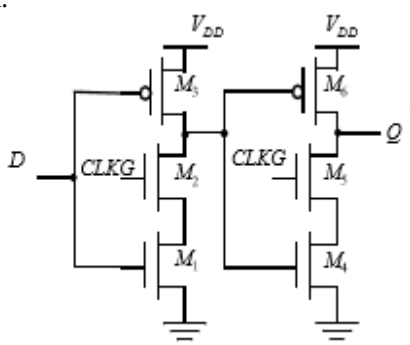

Figure 4: True Single Phase clocked pulsed latch

5. Simulation Results

Fig.5 shows the schematic of conventional method1 PPCFF and Fig.6 shows the simulation results. The PPCFF is a negative edge triggered Master-Slave Data flip-flop. When a clock signal is applied, the output follows the input.

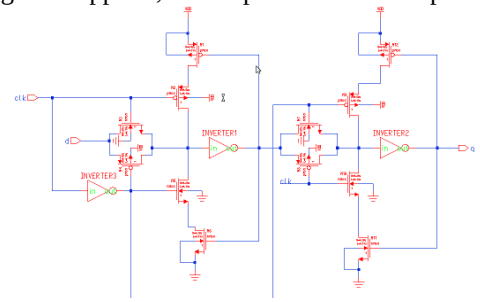

Figure 5: Schematic of conventional method1 PPCFF

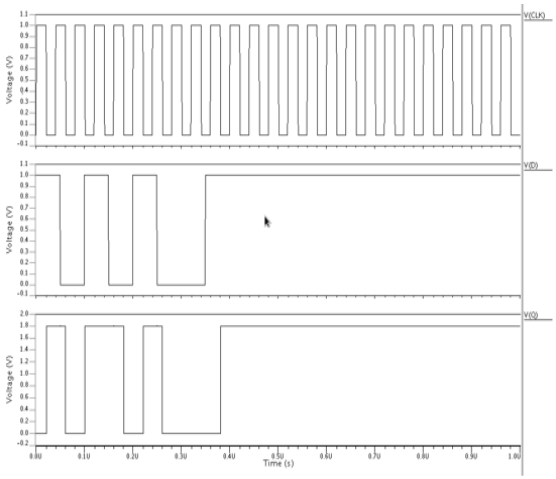

Figure 6: Simulation results of conventional PPCFF Master-slave flip-flop

Fig.7 shows the schematic of conventional method2 SSASPL and Fig.8 showws the simulation results.The SSASPL works like a data flip-flop by using pulsed clock signal instead of full clock signal.The output follows the input at the pulsed clock signal.

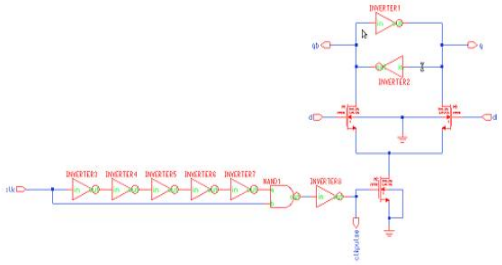

Figure 7: Schematic of conventional method 2 SSASPL Pulsed latch

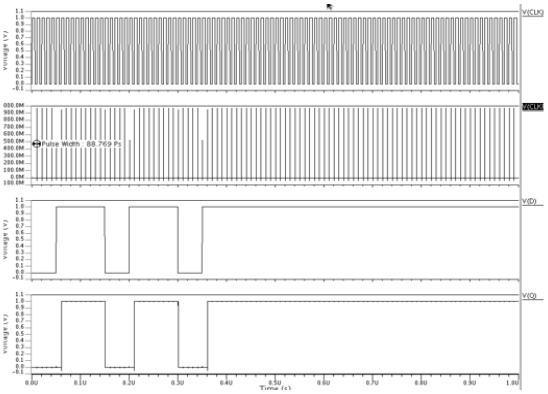

Figure 8: Simulation waveforms of SSASPL pulsed latch

Fig.9. shows the schematic of proposed TSPC pulsed latch , Fig.10 and Fig.11 shows the simulation results and layout. During the pulsed clock signal, output follows the input.

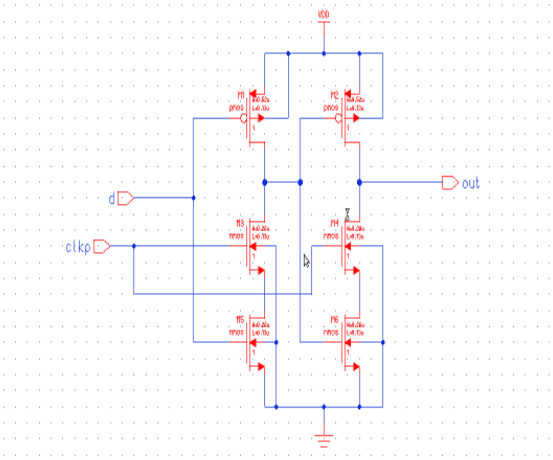

Figure 9: Schematic of proposed TSPC pulsed latch

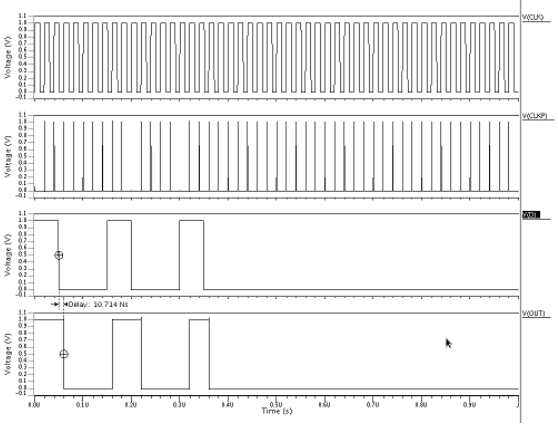

Figure 10: Simulation results of TSPC pulsed latch

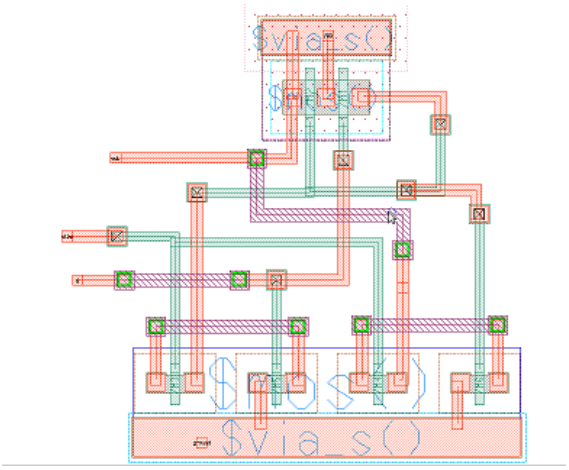

Figure 11: Layout of proposed pulsed latch

Fig.12 shows the schematic of conventional pulsed clock generator by which five on-overlapping clock pulses are geneated.

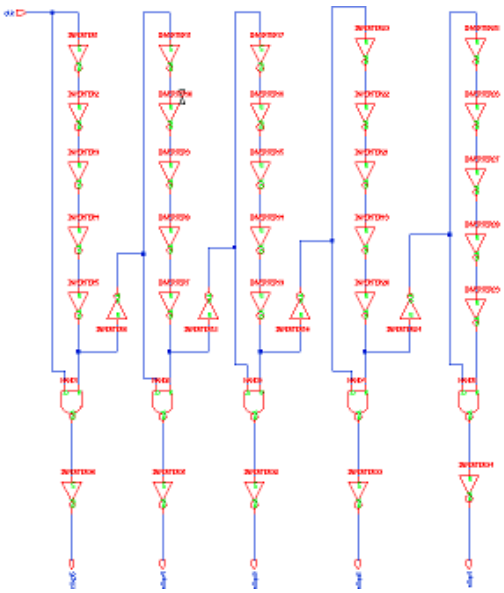

Figure 12: Schematicof conventional clock generator

Fig.13.Shows the schematic of proposed clock generator in which less number of delay cells are used compared to conventional clock generator.

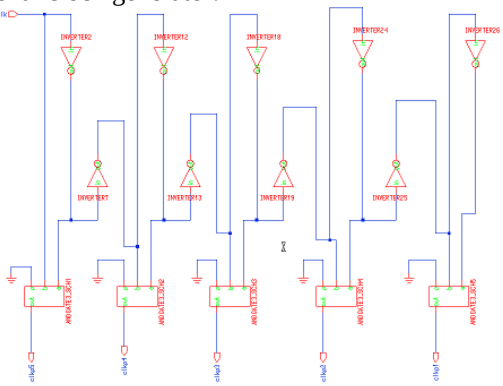

Figure 13: Schematic of proposed clock generator

Fig.14. Shows the simulation results of proposed clock generator with maximum pulse width of 326.10ps and maximum delay between two clock pulses are 294.45ps and the power dissipation of the clock generator is 6.1354nW.

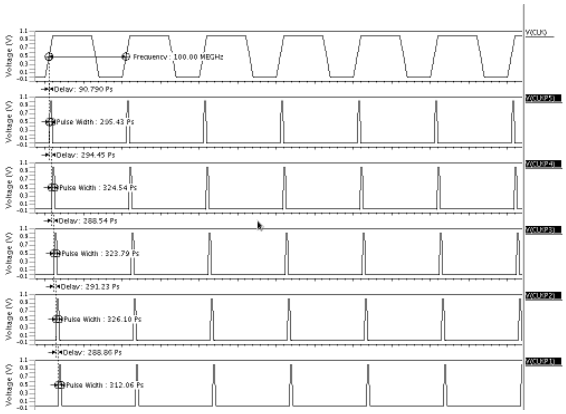

Figure 14: Simulation results of proposed clock generator

Fig.15. Shows the schematic of proposed 4bit shift register and Fig.16. shows the simulation results. The Data input is applied at the input of first latch. According to the pulsed clock signals of the clock generator,the shifting of data takes place.The maximum delay between Q1 and Q4 of 4 bit shift register is 59.134ns.

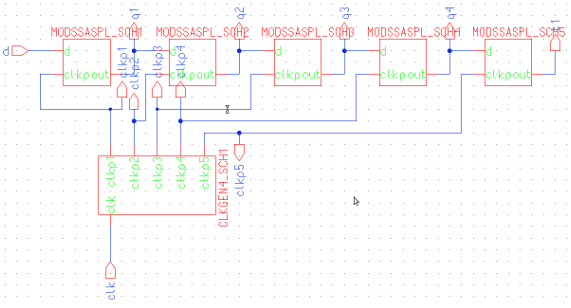

Figure 15: Schematic of proposed 4bit shift register.

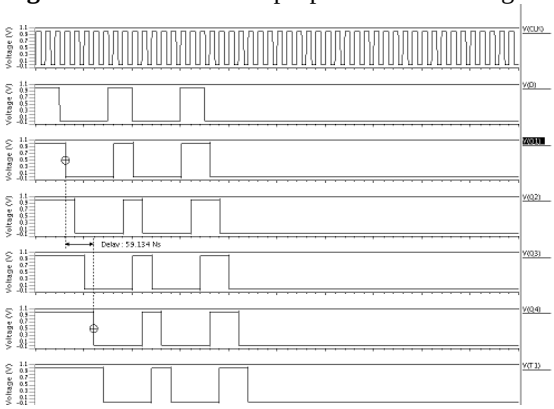

Figure 16: Simulation results of 4 bit shift register using proposed TSPC pulsed latch

Fig.17. shows the schematic of proposed 16 bit shift register and Fig.18. shows its layout design.In the design of shift register using pulsed latches, a single clock pulse cannot reach to all latches of sub shift regi sters or degrading of clock pulses due to parasitic capacitance and resistance.To over come this problem, a clock buffer circuit has to be used.

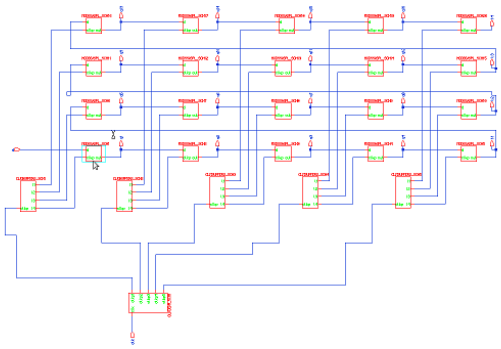

Figure 17: Schematic of proposed 16 bit shift register.

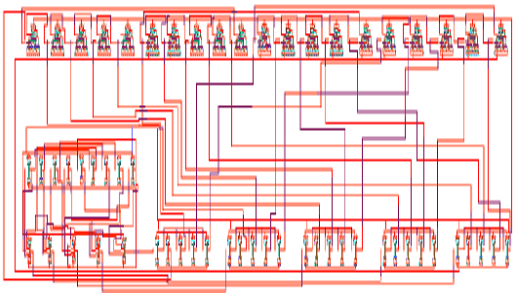

Figure 18: Layout of proposed 16bit shift register.

Fig.19 and Fig.20 shows schematic and simulation waveforms of proposed 64 bit shift register. The maximum delay betweenQ1 and Q64 is 959.14ns.

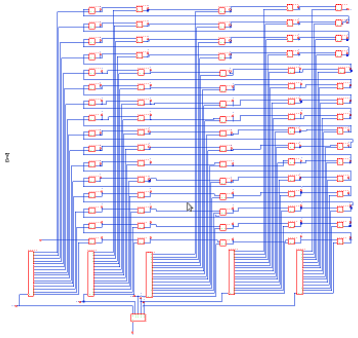

Figure 19: Schematic of proposed 64 bit shift register.

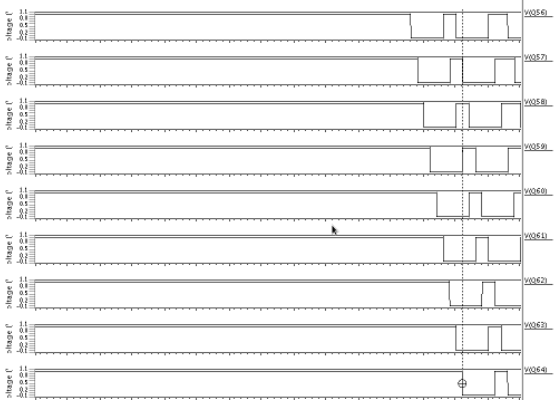

Figure 20: Simulation results of proposed 64 bit shift register.

Fig. 21. shows the schematic of clock buffer circuit used in the designing of shift register to drive the pulsed clock signals without any skew.

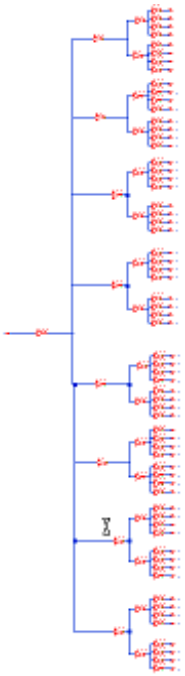

Figure 21: Schematic of clock buffer circuit.

Fig.22. and Fig.23. shows the schematic and simulation results of proposed 128 bit shift register. Shifting of data takes place from Q1 to Q128 in serial manner according to pulsed clock signals.

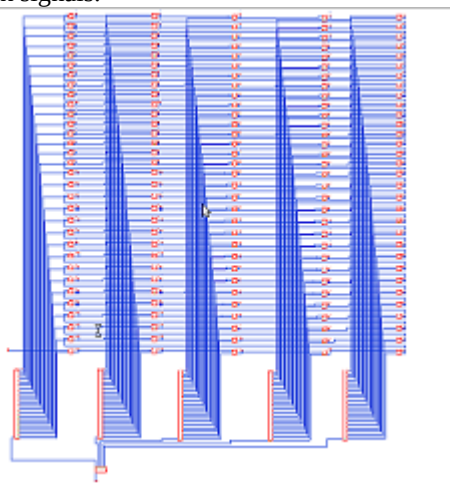

Figure 22: Schematic of proposed 128 bit shift register.

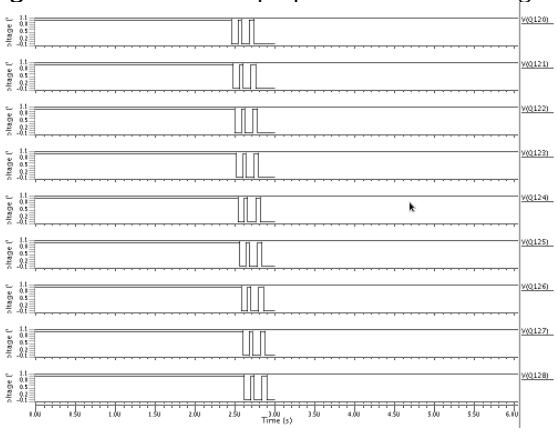

Figure 23: Simulation results of proposed 128 bit shift register.

Fig.24 shows the schematic of proposed 256 bit shift register using TSPC pulsed latches. Five clock buffer circuits are used in the schematic to drive the clock pulses effectively even at the higher bits of shift register.

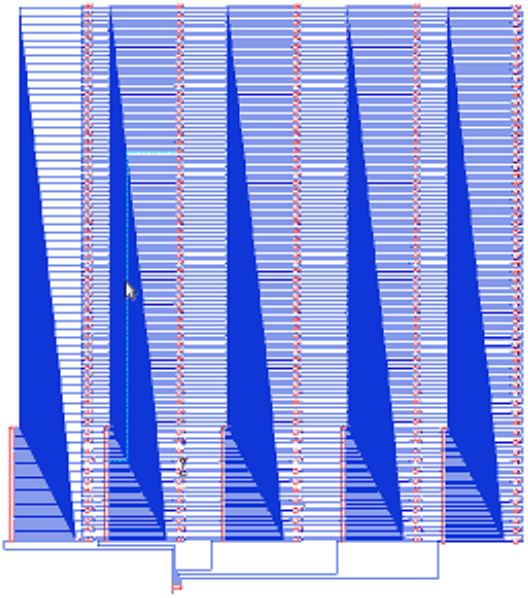

Figure 24: Schematic of proposed 256 bit shift register.

6. Performance comparison in terms of Area and power dissipation.

Table 1shows the transistor comparison of different pulsed latches and flip-flops. Among flip-flops, PPCFF has less number of transistors and in pulsed latches,TSPC has less number of transistors. So shift register using TSPC pulsed latch occupies less areathan other types.

Table1: Transistor comparison between pulsed latches and flip-flops

Different types of pulsed latches and flip-flops		Total no.of transistors
Pulsed latches	**TSPC**[17]	6
	SSASPL [7]	7
	TGPL [8]	12
	HLFF [9]	14
	CP3L [10]	26
Flip-flops	**PPCFF** [11]	16
	SAFF [12]	18
	DMFF [13]	22
	CPSA [14]	28
	CCFF [15]	28
	ACFF [16]	22

Table 2 shows the performance comparison of two conventional methods SSASPL and PPCFF and proposed TSPC pulsed latch. The number of transistors used in proposed TSPC pulsed latch are very less and the power dissipation is also very less compared to conventional method 1 PPCFF and conventional method 2 SSASPL. The number of clock signals used for PPCFF are 8 and 2 for TSPC pulsed latch and only one clock signal for SSASPL.

Table 2: Performance comparison of conventional SSASPL and PPCFF and Proposed TSPC pulsed latch

	PPCFF	SSASPL	TSPC Pulsed latch
Type	Flip-flop	Pulsed latch	Pulsed latch
No. of transistors	16	7	6
clock	8	1	2
Min. clock pulse width (ps)	-	114.32	245.43
Pulsed clock delay (ps)	-	202.17	288.86
Power dissipation (nW)	8.9196	6.8062	2.9000

Table 3 shows the performance comparison of Shift registers of two conventional methods. Using of pulsed latches for designing long bits of shift registers, can reduce usage of clock signal. This is due to the using of same pulsed clock signals to all the latches of Shift register.

Table 3: Performance comparison of Shift registers using conventional SSASPL and PPCFF

Shift register	Power dissipation (nW)	
No. of bits	PPCFF (Flip-flop)	SSASPL (pulsed latch)
4 bit	15.5735	9.5639
8 bit	29.9069	19.1278
16 bit	35.1793	22.1426
32 bit	69.1188	62.2614
64 bit	109.8460	100.6391

The power dissipation of the clock generator circuit used in conventional method 2 Shift register using SSASPL is 24.2101nW. The power dissipation of the clock generator circuit used in proposed Shift register using TSPC pulsed latches is 6.1354nW which is one fourth of the power dissipation of conventional clock generator.The basic AND gate used in the generation of pulsed clock signals in conventional clock generator is replaced by GDI AND gate in proposed clock generatorcircuit and also the number delay cells used are also reduced.

Table 4 shows the performance comparison of Shift register using conventional SSASPL and proposed TSPC pulsed latch in terms of Power dissipation.

Table 4: Performance comparison of Shift registers using conventional SSASPL and proposed TSPC pulsed latch

Shift register	Power dissipation (nW)	
No. of bits	SSASPL	TSPC Pulsed latch
4 bit	33.7740	14.7872
8 bit	43.3379	17.2320
16 bit	46.3527	29.4038
32 bit	86.4715	52.6722
64 bit	165.8492	86.7950

The power dissipation of 128bit shift register using TSPC pulsed latches is 156.1156nW and for 256 bit is 287.8331nW.The power dissipation of the clock generators used in both conventional and proposed shift registers are included in the comparison since both are designed using pulsed latches.

7. Application of Shift registers

Shift registers are used in digital devices like computers as temporary data storage, data transfer, data manipulation and as counters. Shift register as counters are used as digital clocks, frequency countersand binary counters. The 5 bit synchronous counter counts sequentially on every clock pulse, the resulting outputs counts upwards from 0 (00000) to 31 (11111).Therefore, this type of counter is known as 5 bit synchronous up counter. The schematic of 5 bit synchronous up counter using proposed shift register is shown in Fig.25. and Fig.26 are the simulation results of synchronous up counter.

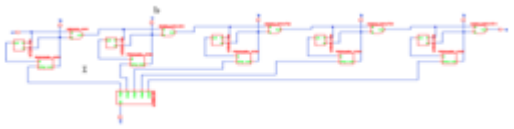

Figure 25: Schematic of 5-bit Synchronous up counter using proposed shift register.

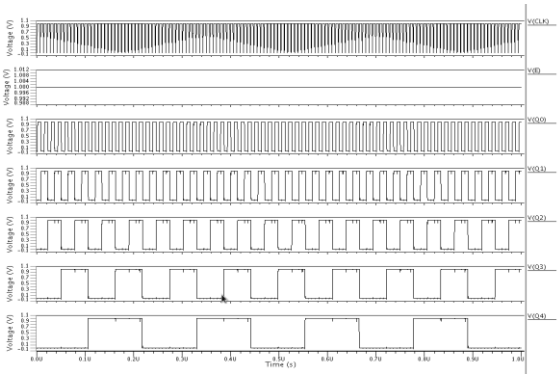

Figure 26: Simulation results of Synchronous up counter

Fig.27. shows the schematic of synchronous up counter using conventional method 2 shift register

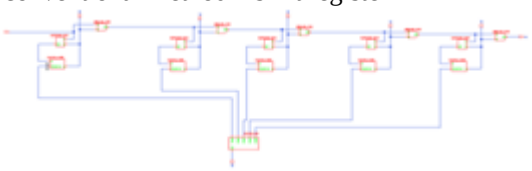

Figure 27: Schematic of Synchronous up counter using conventional method 2 shift register.

Among the Synchronous up counter designed by using two different types of pulsed latch shift registers, power dissipation of the counter designed using TSPC pulsed latch is very less compared to SSASPL which is in micro watts as shown in table 5.

Table 5: Performance comparison f Synchronous up counter using proposed TSPC pulsed latch and conventional SSASPL

Pulsed latch	Power dissipation
SSASPL	31.8882mW
TSPC pulsed latch	15.3434uW

8. Conclusions

Compared to Shift register designed using proposed method with conventional method 1 and method 2, the proposed

method of shift register reduces area and power dissipation. The area was reduced due to the less number of transistors used in the proposed pulsed latch compared to conventional methods. The power dissipation reduced due to the less number of delay cells and GDI AND gate used in the proposed clock generator and also due to the use of less numbered pulsed latch. The shift register was designed in both conventional and proposed methods using 130nm mentor graphics tool.The power dissipation of the shift register using TSPC pulsed latch was reduced to almost half of the shift register using SSASPL pulsed latches.The shift register using proposed TSPC pulsed latchesis compared with the shift register using PPCFF and SSASPL.

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Author Profile

Lakshmi Chinnammalu R pursuing M.Tech. (VLSI) in MVGR College of Engineering (Autonomous), in ECE Department during the academic year 2015-17.

Mr. V. N. Lakshmana Kumar Assistant Professor in ECE department,MVGR College of Engineering (Autonomous), Vizianagaram-535005.